# Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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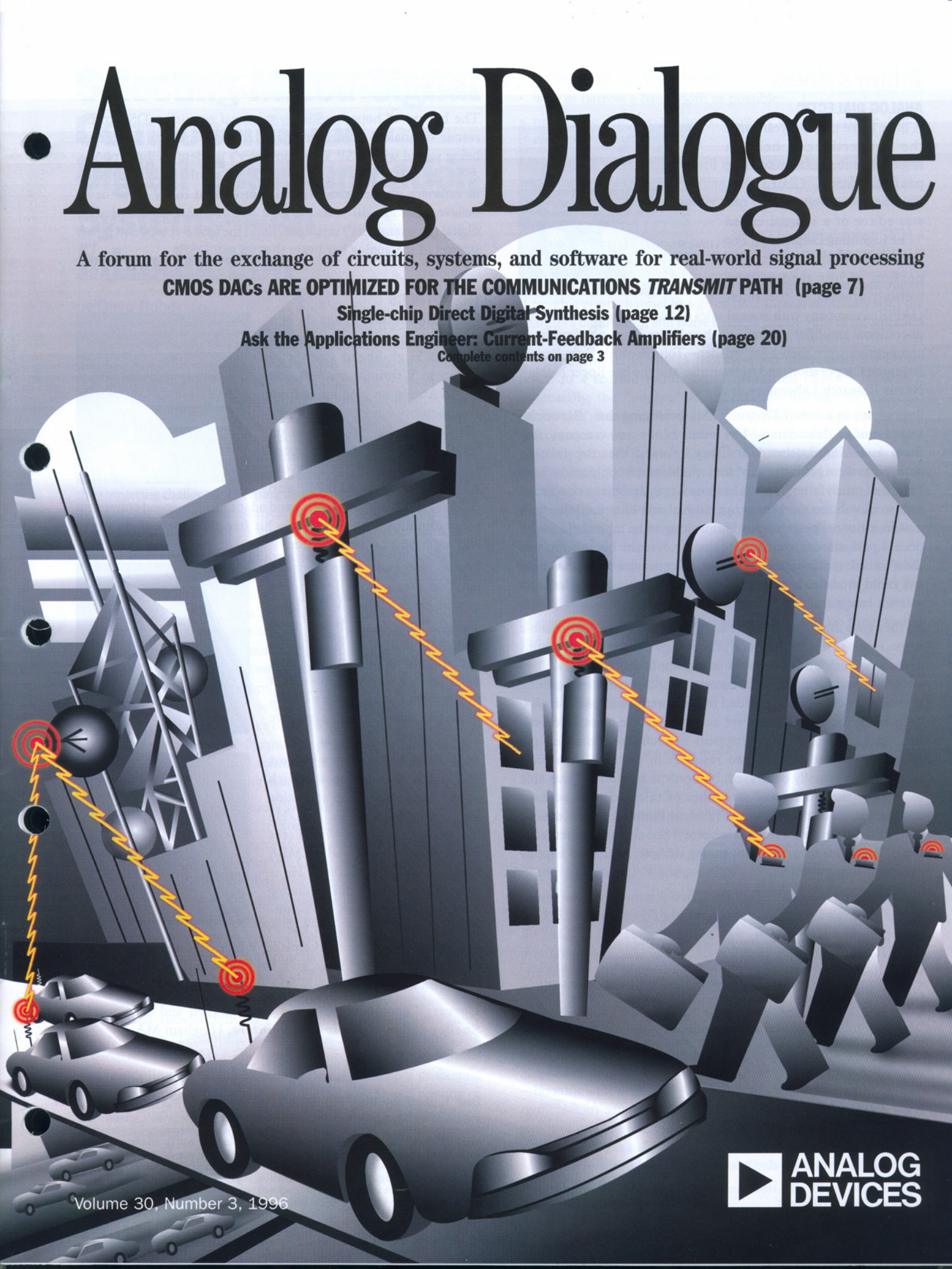

Volume 30, Number 3, 1996

ANALOG DEVICES

# Editor's Notes

## ANALOG DIALECTIC

A little more than 30 years ago, the undersigned held a responsible technical marketing position with George A. Philbrick Researches, Inc., and was editor of a journal called "The Lightning Empiricist." For the edification of a sizeable portion of our readers who weren't around at the time, GAP/R, a company with annual sales of $6M, virtually owned the operational amplifier market—such as it was. The only significant competitors were then a lot smaller—Tom Brown's Burr-Brown Research Corporation, and Al Pearlman and the late Roger Noble's Nexus Research Laboratory, Inc.

Aye, what's in a name? Do you find it interesting that "Research" was part of all three names? The founders of a new company, Ray Stata and Matt Lorber, did. They believed that the existing companies were getting prices* that would interest only researchers (who had much fatter budgets in those days), and that a significant industrial volume market for operational amplifier modules with a wide variety of performance was waiting to be tapped (ICs with decent performance were still pretty far over the horizon, so you didn't need venture capital to buy an expensive fab; you could still build modules in your own garage, or in this case, a loft—or was it a basement?—in Cambridge, MA).

So they gave their company the highly descriptive and serviceable name, Analog Devices, Inc., and offered high-performance op amps at reasonable prices, along with strong application support. They were right, of course! The company's sales took off almost immediately. And ADI was aided by an incredible stroke of luck—both Philbrick and Nexus were acquired by the giant Teledyne, Inc., and merged. As often happens in such circumstances, the effect was like to putting two resistors in parallel; their joint effectiveness actually decreased. Not only that, but ADI was able to acquire the services of a number of talented, and perhaps disgruntled, former employees of Teledyne Philbrick Nexus, a move that proved synergistic. The rest is history! Should the next sentence read: "And with its primacy in analog devices, ADI lived happily ever after?"

Ah, but what's in a name? Don't you find it interesting that one of the fastest-growing product lines at *Analog* Devices is the SHARC general-purpose *digital* signal processor—a DIGITAL COMPUTER, for gosh sakes!? Yes, the analog stuff is doing very well indeed, too, but isn't that a bit of a stretch? If we some day end up getting more revenue from "digital" products than "analog" products, (in no way a sure thing, say our "analog" guys!), will "Analog" in our name be a misnomer?

No! As we're endlessly fond of saying, hardware design problems are *analog* problems. If the name of the game is *signal processing*, any signal that's a voltage or a current—or even a time interval—has resolution limitations that are analog in nature (noise, jitter, bandwidth, etc.), even if the voltage or current level you're trying to recognize is representing a "1" or a "0", and the time is a sampling interval. And don't forget interference: those parasitic spikes the equipment is responding to—or producing—are causing problems an *analog* designer has to solve.

The big ray of hope here is *digital signal processing*. DSP to the rescue of analog! Some very hairy analog problems are indeed being solved with DSP. Your computer's modem, cellular phone, and ac motor controller are doing things via the analog variables in ordinary phone lines, rf, and motors that many of us never believed possible 30 years ago. It's still analog, but it's aided by digital (programmers') intelligence and the space-, cost-, and power savings of the analog hardware that we call DSPs. A

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*For example, the P2 solid-state parametric electrometer was priced at $227 (in mid-1960s US dollars!)

## THE AUTHORS

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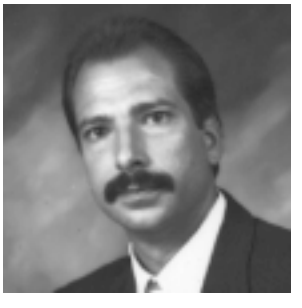

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[*more authors on page 22*]

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# Selecting Mixed-Signal Components for Digital Communication Systems—An Introduction

by Dave Robertson

Communications is about moving information from point A to point B, but the computer revolution is fundamentally changing the nature of communication. Information is increasingly created, manipulated, stored, and transmitted in digital form—even signals that are fundamentally analog. Audio recording/playback, wired telephony, wireless telephony, audio and video broadcast—all of these nominally analog communications media have adopted, or are adopting, digital standards. Entities responsible for providing communications networks, both wired and wireless, are faced with the staggering challenge of keeping up with the exponentially growing demand for digital communications traffic. More and more, communications is about moving *bits* from point A to point B.

Digital communications embraces an enormous variety of applications, with radically different constraints. The transmission medium can be a twisted pair of copper wire, coaxial cable, fiber-optic cable, or wireless—via any number of different frequency bands. The transmission rate can range from a few bits per second for an industrial control signal communicating across a factory floor to 32 kbits/second for compressed voice, 2 Mb/s for MPEG compressed video, 155 Mbps for a SONET data trunk, and beyond. Some transmission schemes are constrained by formal standards, others are free-lance or developmental. The richness of design and architectural alternatives produced by such variety boggles the mind. The digital communications topic is so vast as to defy a comprehensive treatment in anything less than a shelf of books.

A communications jargon and a bewildering array of acronyms have developed, making it sometimes difficult for the communications system engineer and the circuit hardware designer to communicate with one another. Components have often been selected based on voltage-oriented specifications in the time domain for systems whose specifications are expressed in frequency and power. Our purpose here, and in future articles, will be to take a fairly informal overview of some of the fundamentals, with an emphasis on tracing the sometimes complex relationship between component performance and system performance.

The "communications perspective" and analytic tool set have also contributed substantially in solving problems not commonly thought of as "communications" problems. For example, the approach has provided great insight into some of the speed/bandwidth limits inherent in disk-drive data-recovery problems, where the channel from A to B includes the writing and reading of data in a magnetic medium—and in moving data across a high speed bus on a processing board.

**Shannon's law—the fundamental constraint**: In general, the objective of a digital communications system is:

- to move as much data as possible per second
- across the designated channel
- with as narrow a bandwidth as possible
- using the cheapest, lowest-power, smallest-space (etc.) equipment available.

System designers are concerned with each of these dimensions to different degrees. Claude Shannon, in 1948, established the theoretical limit on how rapidly data can be communicated:

This means that the maximum information that can be transmitted through a given channel in a given time increases linearly with the channel's bandwidth, and noise reduces the amount of information that can be effectively transmitted in a given bandwidth, but with a logarithmic sensitivity (a thousandfold increase in noise may result in a tenfold reduction in maximum channel capacity). Essentially, the "bucket" of information has two dimensions: bandwidth and signal-to-noise ratio (SNR). For a given capacity requirement, one could use a wide-bandwidth channel with relatively poor SNR, or a narrowband channel with relatively good SNR (Figure 1). In situations where bandwidth is plentiful, it is common to use cheap, bandwidth-hungry communications schemes because they tend to be insensitive to noise and implementation imperfections. However, as demand for data communication capacity increases (e.g., more cellular phones) bandwidth is becoming increasingly scarce. The trend in most systems is towards greater spectral efficiency, or bits capacity per unit of bandwidth used. By Shannon's law, this suggests moving to systems with better SNR and greater demands on the transmit and receive hardware and software.

Let's examine the dimensions of bandwidth (time/frequency domain) and SNR (voltage/power domain) a little more closely by considering some examples.

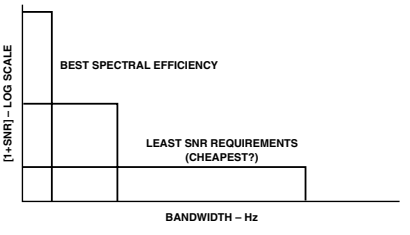


Figure 1. Shannon's capacity limit: equal theoretical capacity.

## IN THIS ISSUE

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**PCM: A simple (but common) case:** Consider the simple case of transmitting the bit stream illustrated in Figure 2a, from a transmitter at location A to a receiver at location B (one may assume, that the transmission is via a pair of wires, though it could be any medium.) We will also assume that the transmitter and receiver have agreed upon both the voltage levels to be transmitted and the timing of the transmitted signals. The transmitter sends "high" and "low" voltages at the agreed-upon times, corresponding to 1s and 0s in its bit stream. The receiver applies a decision element (comparator) at the agreed-upon time to discriminate between a transmitted "high" and "low", thereby recovering the transmitted bit stream. This scheme is called *pulse code modulation* (or PCM). Application of the decision element is often referred to as "slicing" the input signal stream, since a determination of what bit is being sent is based on the value of the received signal at one instant in (slice of) time. To transmit more information down this wire, the transmitter increases the rate at which it updates its output signal, with the receiver increasing its "slicing" rate correspondingly.

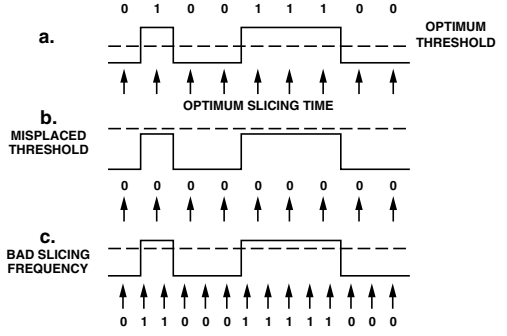



Figure 2. Simplified bit voltage transmission (PCM).

This simple case, familiar to anyone who has had an introductory course in digital circuit design, reveals several of the important elements in establishing a digital communications system. First, the transmitter and receiver must agree upon the "levels" that are to be transmitted: in this case, what voltage constitutes a transmitted "1", and what voltage level constitutes a transmitted "0". This allows the receiver to select the right threshold for its decision element; incorrect setting of this threshold means that the transmitted data will not be recovered (Figure 2b). Second, the transmitter and receiver must agree on the transmission frequency; if the receiver "slices" at a different rate than the bits are being transmitted, the correct bit sequence will not be recovered (2c). In fact, as we'll see in a moment, there must be agreement on both frequency and phase of the transmitted signal.

How difficult are these needs to implement? In a simplified world, one could assume that the transmitted signal is fairly "busy", without long strings of consecutive ones or zeros. The decision threshold could then be set at the "average" value of the incoming bit stream, which should be some value between the transmitted "1" and transmitted "0" (half-way between, if the density of ones and zeros are equal.) For timing, a phase-locked loop could be used—with a center frequency somewhere near the agreed-upon transmit frequency; it would "lock on" to the transmitted signal, thereby giving us an exact frequency to slice at. This process is usually called *clock recovery*; the format requirements on the transmit signal are related to the performance characteristics of the phase-locked-loop. Figure 3 illustrates the elements of this simplified pulse receiver.

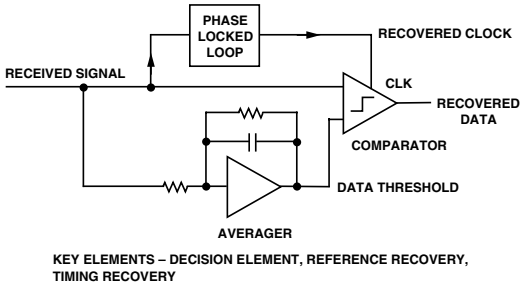



Figure 3. Idealized PCM.

**Bandwidth Limitations:** The real world is not quite so simple. One of the first important physical limitations to consider is that the transmission channel has finite bandwidth. Sharp-edged square wave pulses sent from the transmitter will be "rounded off" by a low bandwidth channel. The severity of this effect is a function of

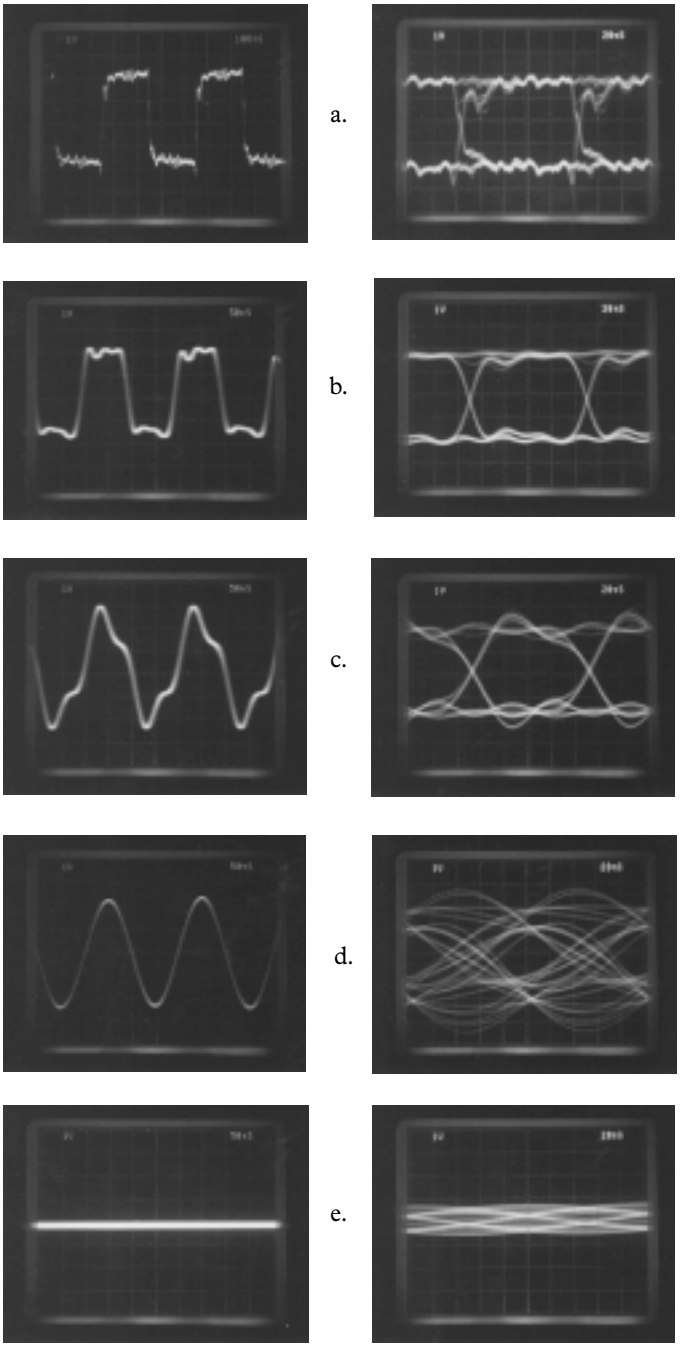



Figure 4. Scope waveforms vs. time (L) and eye diagrams (R).

the channel bandwidth. (Figure 4). In the extreme case, the transmitted signal never gets to a logical "1" or "0", and the transmitted information is essentially lost. Another way of viewing this problem is to consider the impulse response of the channel. An infinite bandwidth channel passes an impulse undistorted (perhaps with just a pure time delay). As the bandwidth starts to decrease, the impulse response "spreads out". If we consider the bit signal to be a stream of impulses, inter-symbol interference (ISI) starts to appear; the impulses start to interfere with one-another as the response from one pulse extends into the next pulse. The voltage seen at the Receive end of the wire is no longer a simple function of the bit sent by the transmitter at time $t_1$, but is also dependent on the previous bit (sent at time $t_0$), and the following bit (sent at time $t_2$).

Figure 4 illustrates what might be seen with an oscilloscope connected to the Receive end of the line in the simple noisy communications system described above for the case where the bandwidth restriction is a first-order lag (single R-C). Two kinds of response are shown, a portion of the actual received pulse train and a plot triggered on each cycle so that the responses are all overlaid. This latter, known as an "eye" diagram, combines information about both bandwidth and noise; if the "eye" is open sufficiently for all traces, 1s can be easily distinguished from 0s. In the adequate bandwidth case of Figure 4a, one can see unambiguous 1s, 0s, and sharp transitions from 1 to 0. As the bandwidth is progressively reduced, (4b, 4c, 4d, 4e), the 1s and 0s start to collapse towards one another, increasing both timing- and voltage uncertainty. In reduced-bandwidth and/or excessive-noise cases, the bits bleed into one another, making it difficult to distinguish 1s from 0s; the "eye" is said to be *closed* (4e).

As one would expect, it is much easier to design a circuit to recover the bits from a signal like 4a than from 4d or 4e. Any misplacement of the decision element, either in threshold level or timing, will be disastrous in the bandlimited cases (d, e), while the wideband case would be fairly tolerant of such errors. As a rule of thumb, to send a pulse stream at rate $F_S$, a bandwidth of at least $F_S/2$ will be needed to maintain an open eye, and typically wider bandwidths will be used. This *excess bandwidth* is defined by the ratio of actual bandwidth to $F_S/2$. The bandwidth available is typically limited by the communication medium being used (whether 2000 ft. of twisted-pair wire, 10 mi of coaxial cable etc.), but it is also necessary to ensure that the signal processing circuitry in the transmitter and receiver do not limit the bandwidth.

Signal processing circuitry can often be used to help mitigate the effects of the intersymbol interference introduced by the bandlimited channel. Figure 5 shows a simplified block diagram of a bandlimited channel followed by an equalizer, followed by the bit "slicer". The goal of the equalizer is to implement a transfer function that is effectively the inverse of the transmission channel over a portion of the band to extend the bandwidth. For example, if the transmission channel is acting as a low pass filter, the equalizer might implement a high-pass characteristic, such that a signal passing through the two elements will come out of the equalizer undistorted over a wider bandwidth.

Though straightforward in principle, this can be very difficult to implement in practice. To begin with, the transfer function of the transmission channel is not generally known with any great precision, nor is it constant from one situation to the next. (You and your neighbor down the street have different length phone wires running back to the phone company central office, and will therefore have slightly different bandwidths.) This means that these equalizers usually must be tunable or adaptive in some way. Furthermore, considering Figure 5 further, we see that a passive equalizer may flatten out the frequency response, but will also attenuate the signal. The signal can be re-amplified, but with a probable deterioration in signal-to-noise ratio. The ramifications of that approach will be considered in the next section. While they are not an easy cure-all, equalizers are an important part of many communications systems, particularly those seeking the maximum possible bit rate over a bandwidth-constrained channel. There are extremely sophisticated equalization schemes in use today, including decision feedback equalizers which, as their name suggests, use feedback from the output of the decision element to the equalization block in an attempt to eliminate trailing-edge intersymbol interference.[1]

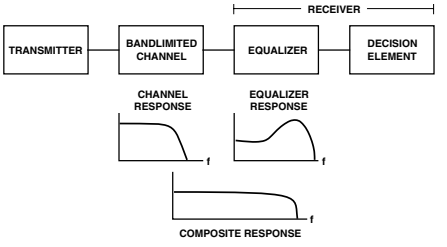



Figure 5. Channel equalization.

**Multi-level symbols—sending more than one bit at a time:** Since the bandwidth limit sets an upper bound on the number of pulses per second that can be effectively transmitted down the line, one could decide to get more data down the channel by transmitting two bits at a time. Instead of transmitting a "0" or "1" in a binary system, one might transmit and receive 4 distinct states, corresponding to a "0" (00), "1" (01), "2" (10), or "3" (11). The transmitter could be a simple 2-bit DAC, and the receiver could be a 2-bit ADC. (Figure 6). In this kind of modulation, called pulse-amplitude modulation (PAM), additional information has been encoded in the amplitude of the bit stream.

Communication is no longer one bit at a time; multiple-bit words, or *symbols*, are being sent with each transmission event. It is then necessary to distinguish between the system's bit rate, or number of bits transmitted per second, and its symbol rate, or baud rate, which is the number of *symbols* transmitted per second. These two rates are simply related:

$$bit\ rate = symbol\ rate\ (\text{baud}) \times bits/symbol$$

The bandwidth limitations and intersymbol interference discussed in the last section put a limit on the realizable symbol rate, since they limit how closely spaced the "transmission events" can be in time. However, by sending multiple bits per symbol, one can increase the effective bit rate, employing a *higher-order modulation* scheme. The transmitter and receiver become significantly more complicated. The simple switch at the transmitter has now been replaced with a DAC, and the single comparator in the receiver is

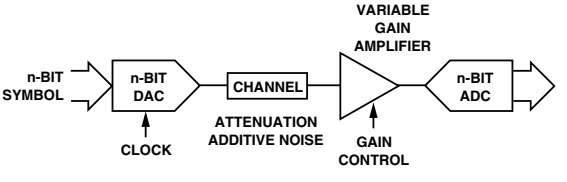



Figure 6. Simplified PAM transmitter/receiver.

[1]The field of disk-drive *read*-channel design is a hotbed of equalizer development in the ongoing struggle to improve access specs.

now an A/D converter. Furthermore, it is necessary to use more care to properly scale the amplitude of the received signal; more information is needed than just the sign. Making the simplifying assumption that the A/D converter, representing the receiver, is implemented as a straight flash converter, it is manifest that the receiver hardware complexity grows exponentially with the number of bits per symbol: one bit, one comparator; two bits, 3 comparators; three bits, 7 comparators, etc. Depending on the particular application, circuit cost should not quite increase exponentially with bits per symbol, but it generally will be a steeper-than-linear increase. However, hardware complexity is not the only limiting factor on the number of bits per symbol that can be transmitted.

**NOISE LIMITATIONS**

Consider again the simple case of one-bit-per-symbol PCM modulation. Assuming that 1 V is used to send a "1", and –1 V to send a "0", the simple receiver (Figure 3) is a comparator with its decision threshold at 0 V. In the case where the bit being received is a "0", and the channel bandwidth is wide enough so that there is virtually no intersymbol interference, in a noiseless environment, the voltage at the receiver is expected to be –1 V. Now introduce additive noise to the received signal (this could come from any number of sources, but for simplicity and generality, assume it to be gaussian white noise that could correspond to thermal noise). At the moment the decision element is applied, the voltage at the comparator will differ from –1 V by the additive noise. The noise will not be of real concern unless it contains values that will push the voltage level above 0 V. If the noise is large enough (and in the right sign) to do this, the decision element will respond that it has received a "1", producing a bit error. *In the eye diagram of Figure 4d, the noise would produce occasional closures of the "eye".*

If the system is modified to send a 4-bit (16-level) symbol, with the same peak-to-peak voltage, –1 V corresponds to "0" (0000), and +1 V corresponds to "15" (1111). Now the incremental threshold between "0" and the next higher level, "1", is much smaller: 16 distinct states must fit into the 2-V span, so the states will be roughly 125 mV apart, center-to-center. If the decision thresholds are placed optimally, the "center" of a state will be 62.5 mV away from adjacent thresholds. In this case, >62.5 mV of noise will cause a "bit error". If the initial assumption holds and the additive noise is gaussian in nature, one can predict from the rms noise value how often the noise will exceed this critical value. Figure 7 shows the error threshold of 62.5 mV for the probability density functions of two different rms noise values. From this, one can predict the bit error rate, or how often the received data will be interpreted incorrectly for a given transmitted bit rate.

Special care must be taken as to how the data is encoded: if the code 1000 is one threshold away from the code 0111, a small noise excursion would actually cause all 4 bits to be misinterpreted. For this reason, Gray code (which changes only one bit at a time between adjacent states—e.g., 00, 01, 11, 10) is often used to minimize the bit error impact from a misinterpretation between two adjacent states.

So, despite the increase in bit rate, there are limitations to using higher-order modulation schemes employing more bits per symbol: not only will the hardware become more complex, but, for a given noise level, bit errors will be more frequent. Whether the bit error rate is tolerable depends very much on the application; a digitized voice signal may sound reasonable with a bit error rate of $10^{-5}$, while a critical image transmission might require $10^{-15}$.

Bit errors can be detected and corrected by various coding and parity schemes, but the overhead introduced by these schemes eventually consumes the additional bit capacity gained from increasing the symbol size. One way to try to increase the signal-to-noise ratio (SNR) is to increase transmitted power; for example, increase signal amplitude from 2 V peak-to-peak to 20 V peak-to-peak, thereby increasing the "error threshold" to 625 mV. Unfortunately, increasing the transmitted power generally adds to the cost of the system. In many cases, the maximum power that can be transmitted in a given channel may be limited by regulatory authorities for safety reasons or to ensure that other services using the same or neighboring channels are not disturbed. Nevertheless, in systems that are straining to make use of all available capacity, the transmit power levels will generally be pushed to the maximum practical/legal levels.

Voltage noise is not the only kind of signal impairment that can degrade the receiver performance. If timing noise, or jitter, is introduced into the receiver "clock," the decision "slicer" will be applied at sub-optimal times, narrowing the "eye" (Figs. 4a-4d) horizontally. Depending on how close the channel is to being band-limited, this could significantly decrease the "error threshold," with increased sensitivity to voltage noise. Hence, SNR must be determined from the combination of voltage-domain and time-domain error sources.

*This is the first in a series of articles offering an introduction to topics in communications. In the next issue, we'll discuss various modulation schemes and ways of multiplexing multiple users in the same channel.* A

**For Further Reading:** This article scratches the surface of a very complex field. If your appetite for information has been whetted, here are a few suggested texts (bibliographies within these books will fan out to a wider list):

*Electronic Communication Systems—a complete course*, 2nd edition, by William Schweber. Englewood Cliffs, NJ: Prentice Hall ©1994. A good basic introduction to communications fundamentals, with an emphasis on intuitive understanding and real-world examples. No more than one equation per page.

*Digital Communication* (2nd edition), by Edward Lee and David Messerschmitt. Norwell, MA: Kluwer Publishing, ©1994. A more comprehensive and analytical treatment of digital communications.

*Wireless Digital Communications: Modulation and Spread-Spectrum Applications*, by Dr. Kamilo Feher. Englewood Cliffs, NJ: Prentice Hall, ©1995. A fairly rigorous analysis of different wireless modulation schemes, with insights into particular strengths and weaknesses of each, and discussion of why particular schemes were chosen for certain standards.

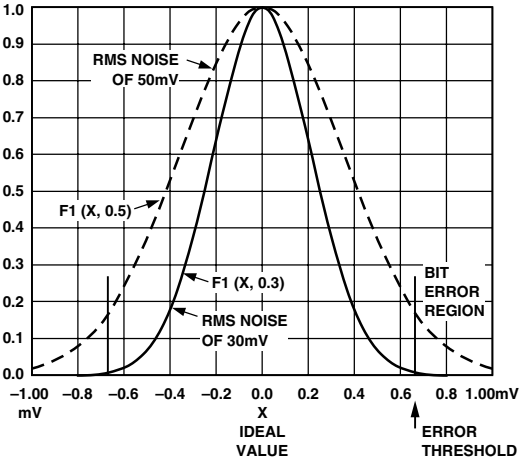



Figure 7. Ideal signal plus noise vs. error threshold: Threshold at 2 σ, and threshold at 1 σ.

# DACs are Optimized for Communication *Transmit* Path

## High-speed CMOS TxDAC™ 8-to-14-bit family with clock rates up to 125 MSPS

by Doug Mercer and Joe DiPilato

The pin-compatible AD976x family of 8-, 10-, 12-, and 14-bit TxDAC™ low-distortion DACs offers excellent spurious-free dynamic range (SFDR) specs at clock rates of up to 125 MSPS with the low price and power levels typical of CMOS devices.

The rapidly expanding consumer-oriented wireless and wireline communications markets have fostered an insatiable demand for high-speed analog-to-digital and digital-to-analog converters having good dynamic (frequency-domain) performance at low cost and with low power dissipation. The most visible manifestation has been the feast of new CMOS ADC offerings developed to meet the needs of the *receive* path; but there's been a lack of choice of low-cost CMOS DAC products with dynamic performance suitable for many *transmit* signal-path applications.

Traditional time-domain and dc linearity characteristics, such as integral nonlinearity (INL), differential nonlinearity (DNL), glitch impulse, and settling time are not adequate indicators of response and distortion in the frequency domain. Most existing high-speed CMOS DACs, developed primarily for video applications, tend to have poor spurious-free dynamic range (SFDR) and harmonic distortion (THD). Bipolar and BiCMOS devices can provide the required dynamic performance, but they are usually too costly, require dual supplies, and use too much power to be suitable for tomorrow's high-volume communications applications.

The low-power requirement is driven by communications-platform changes. They are either getting physically smaller and require higher component packaging density (e.g., micro and pico basestations packaged in small boxes that hang off telephone poles and sides of buildings); or are portable and battery-operated (for example, telephones, pagers, meter-reading terminals, etc.); or are powered by telephone lines (wireless local loop); or require battery back-ups (telephony over cable, life-line services). These requirements all dictate low power for extended battery life, minimized heat dissipation, and ability to operate with limited power available. In this regard, single-supply components avoid the cost and inefficiency of additional supplies. 3-V single-supply devices are becoming very popular to achieve even lower power dissipation and compatibility with high density digital circuits.

These requirements for low cost and low power with good dynamic performance have led to the development of a new class of high-speed CMOS DACs for transmit applications. This new low-cost TxDAC™ family, specified to operate at update rates of up to 125 MHz, represents a major break-through for high-speed transmit-path CMOS DACs. They offer SFDR performance that, until now, was simply unobtainable with high-speed CMOS DACs.

The first five members of the TxDAC family include the *8-bit, 50-MSPS* AD9708AR; the *10-bit, 50-MSPS* AD9760AR-50; the *10-bit, 125-MSPS* AD9760AR; the *12-bit, 125-MSPS* AD9762AR; and the *14-bit, 125MSPS* AD9764AR. All five models are offered in pin-compatible 28-pin SOIC packages, allowing designers to make easy price/performance trade-offs during the evaluation stages of the design cycle. Figure 1 shows a functional block diagram of the 12-bit AD9762 and the pin-out of the 10-bit AD9760. The MSB (DB *N*–1) is always pin-1 in this family, irrespective of the resolution; lower-resolution devices can be directly connected to circuits wired for higher-resolution devices. This permits a uniform design footprint and the direct swapping of different-resolution models for comparison, upgrading, and downpricing.

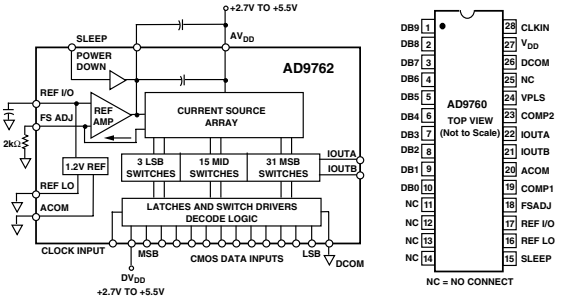



Figure 1. AD9762 block diagram and AD9760 pinout.

These devices are fabricated on a low-cost sub-micron single-polysilicon double-metal CMOS process. Each DAC's analog and digital circuitry can operate from single +2.7 V to +5.5 V supplies (providing full 3-V, single-supply operation). Each DAC includes a temperature-compensated 1.2-V band-gap reference and provides differential current outputs up to 20 mA full-scale (compliance voltage = 1.25 V), regulated by an on-chip reference amplifier, and settable anywhere from 2 mA to 20 mA, using an external resistor. The DAC outputs settle to within 0.25% of final value within 35 ns. Rise and fall times from 10% to 90% of full scale are specified at 2.5 ns, and output propagation delay is only 1 ns.

### DESIGN FEATURES

To eliminate amplitude-dependent distortion associated with traditional R-2R ladder architectures, and for superior ac and dc performance, the TxDACs employ segmented current sources. For example, at the core of the 12-bit AD9762 are 49 current sources (Figure 1). The 5-most-significant-bits' contribution to the output is formed by summing up to 31 equal current sources, each having a weight of $2^{-5}$ FS. The contribution of the next four bits is provided by summing up to 15 current sources with 1/16th the weight of the first set (i.e., $2^{-9}$ FS each). The 3 LSBs are formed by a more-or-less conventional 3-bit binary DAC switching currents with weights of 1/2, 1/4, and 1/8 of the second set. This segmentation architecture is the key to the AD9762's achieving its ±0.5 LSB 12-bit DNL performance and its low 5 pV-s output glitch-impulse spec, as well as its excellent SFDR in multi-tone applications, where the output of the DAC is normally operating at 1/2 or 1/4 full-scale. Figure 2 shows AD9762's single-tone SFDR vs. output level at various rates.

For use in the *transmit* path of communications applications, the segmented current-source architecture was by itself insufficient to achieve the required SFDRs. To reduce the inherent causes of ac distortion, especially even harmonics, intense design effort was focused on improving output switch timing. The resulting innovative proprietary latch and switch circuitry has produced an SFDR increase of approximately 20 dB over traditional CMOS "video" DAC offerings. What's more, the TxDAC family's SFDR performance is comparable to that of the best bipolar and BiCMOS IC devices, but at a fraction of the power and price.

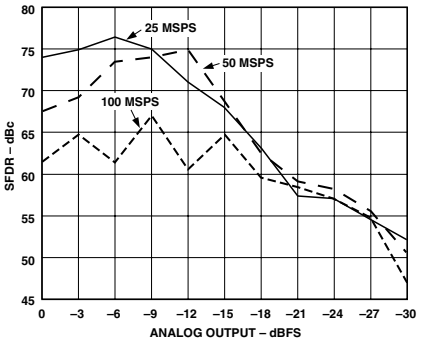



Figure 2. SFDR vs. output amplitude at various sampling rates.

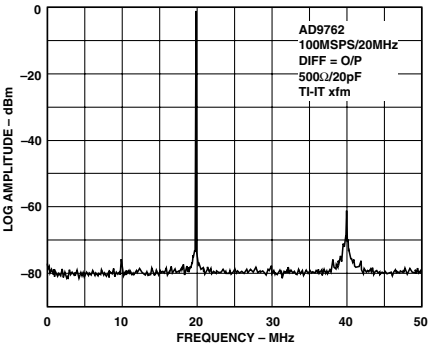



Figure 3. 19.96-MHz sine wave sampled at 100 MSPS; differential output, 50 Ω, 20 pF, SFDR = 60.8 dB.

## SPURIOUS-FREE DYNAMIC RANGE

Why is SFDR important in communications? Usually, the information being transferred shares the frequency spectrum/bandwidth with other communication channels and applications (for example, different television channels being broadcast or transmitted by a common cable, different callers in a cellular system, different FM radio stations, etc.) If a transmitter sends spurious signals into other frequency bands, they can corrupt, interrupt, or obliterate the neighboring signal(s). This is considered to be bad practice, is counter to the regulations of the FCC (and other regulatory bodies), and can lead to legal action.

The TxDAC family has SFDRs over the Nyquist band upwards from 57 dB, when clocked at 100 MSPS and producing a 40-MHz output signal (10-bit AD9760), to 78 dB, when clocked at 20 MSPS and producing a 2-MHz output (14-bit AD9764). Table 1 shows typical SFDR and THD specifications for the AD9760, AD9762, and AD9764 at various clock rates and output frequencies. Though the 12- and 14-bit devices offer similar SFDR for full-scale sine waves, the higher-resolution devices have better SFDR for signals with high peak-to-average ratios and significant low-level content. Figure 3 demonstrates a typical spectral plot over the Nyquist range of the 12-bit AD9762 with an output consisting of a single 20-MHz signal at a 100-MSPS clock rate; shown is a –60.8-dB second harmonic, with the remaining spurs <–75 dB. In most narrow-band applications, the harmonics are filtered out, and the SFDR within "a window" or "without harmonics" is what matters. In this case, the TxDAC family offers performance in the 80-dB range, even for the 10-bit AD9760, for outputs in the 5-MHz range clocked at 100 MSPS.

In wideband applications, where the DAC will be producing several signals at its output, two-tone or multi-tone performance is of especial interest. A salient application is where two or more data/voice/video channels are simultaneously sent down a cable. Wideband cellular basestations is another, and beyond that there are applications like ADSL (Asymmetric Digital Subscriber Line), which utilize discrete multi-tone based modulation schemes and depend on good multi-tone performance.

**Table 1. Typical SFDR and THD specifications**

| **SFDR** | **AD9760** | **AD9762** | **AD9764** |
|---|---|---|---|
| $F_c$=50 MHz; $F_{out}$=5.05 MHz to Nyquist | 67 dBc | 70 dBc | 70 dBc |
| $F_c$=50 MHz; $F_{out}$=20.2 MHz to Nyquist | 64 dBc | 67 dBc | 67 dBc |
| $F_c$=100 MHz; $F_{out}$=5.05 MHz to Nyquist | 61 dBc | 64 dBc | 64 dBc |
| $F_c$=100 MHz; $F_{out}$=40.4 MHz to Nyquist | 57 dBc | 60 dBc | 60 dBc |
| $F_c$=50 MHz; $F_{out}$=5.05 MHz; 2 MHz Span | 84 dBc | 84 dBc | 84 dBc |
| $F_c$=100 MHz; $F_{out}$=5.05 MHz; 2 MHz Span | 84 dBc | 84 dBc | 84 dBc |
| **THD** | | | |
| $F_c$=50 MHz; $F_{out}$=5.05 MHz | –61 dBc | –64 dBc | –64 dBc |
| $F_c$=100 MHz; $F_{out}$=5.05 MHz | –57 dBc | –60 dBc | –60 dBc |

In most multi-tone applications, the output of the transmit-path DAC is normally operated at a fraction of the full-scale range (e.g., 1/2 or 1/4 FS), to ensure that the DAC output doesn't clip with all channels near full-scale (the harmonics produced by clipped transmit waveforms can result in illegal "splatter"). Figures 4 and 5 show spectral plots of an 8-tone waveform at full scale and half-scale, respectively, for the AD9764; both indicate SFDRs > 70 dBc—an important result of the innovative converter architecture. Various models of the TxDAC family have been measured against BiCMOS DACs performing comparably in single-tone tests; the TxDACs achieve repeatably better performance in multi-tone applications. This can be linked to timing skew attributed to the widely used R-2R ladder-network architecture—skews which the TxDACs' proprietary current-switching architecture has been optimized to minimize.

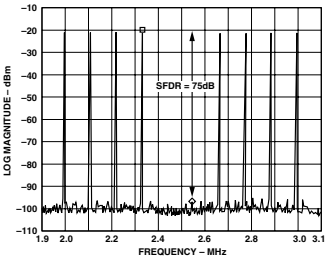



Figure 4. AD9764 8-tone FFT plot, at full-scale output.

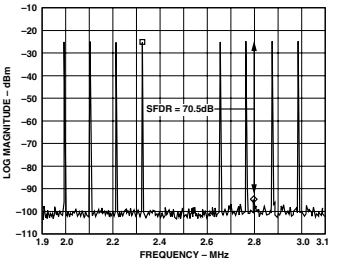



Figure 5. AD9764 8-tone FFT plot, at 1/2-scale output.

The switching circuitry used in the TxDAC core provides true differential outputs, for improved performance when the devices are used differentially. Even though the TxDAC families' single-ended performance is outstanding in its own right, the best possible harmonic performance is achieved when the outputs are driven differentially through a transformer. Table 2 demonstrates the improvement in differential performance over single-ended for the 12-bit AD9762, especially at higher frequencies.

**Table 2. AD9762 Spurious-Free Dynamic Range, Fs = 125 MSPS**

| **One Tone** | **Single-Ended** | **Differential** |
|---|---|---|
| 1 MHz | 70 dBc | 72 dBc |
| 5 MHz | 63 dBc | 70 dBc |
| 10 MHz | 58 dBc | 65 dBc |
| 39 MHz | 46 dBc | 54 dBc |

Each DAC consumes 150 mW when powered from a single +5-V supply and clocked at 100 MSPS, while configured for a 20-mA full-scale current output. The dissipation is reduced to a very low 35 mW when clocked at 40 MSPS, operating from a single +3-V

supply, and configured for 2-mA full-scale output. Each device supports a *sleep* mode, reducing power consumption to < 30 mW (from +5 V) when the DAC is not in operation.

In many cases, the figure of merit in a digital communications system is its bit-error rate (BER). The BER is usually dictated by the appropriate standard/specification, and is affected by a combination of analog component performance, transmission medium, modulation scheme, data rate, and available equalization and error-correction circuitry. The variety of different wireless and wireline applications (including wireless base stations and terminals for cellular, PCS, pager, wireless local loop and satellite services, and wireline modems for Internet access, interactive video set-top box, and digital subscriber lines such as ADSL, HDSL, VDSL, etc.) use many different modulation schemes, accommodate different data rates, and require differing system-level performance.

In these circumstances, the lack of a unique relationship to DAC performance makes it difficult for a communications system designer to establish the converter's required resolution/dynamic range. Fortunately, the TxDACs' pin-compatible footprint permits price-performance trade-offs at any stage of the development cycle, and provides an upgrade path to future higher-performance systems. The system designer has the flexibility to trade off BER performance for system cost. The choice permits the designer to accommodate a certain margin of error, compensating for equalization and error-correction methods and performance. Also, since data rate for a given modulation scheme is proportional to bandwidth and dynamic range, a designer can provide for increased data rates on higher-end devices.

Two basic transmit architectures are shown in Figures 6 and 7. In quadrature-based modulation schemes, such as QPSK and QAM, mixers are deployed to mix the in-phase (I) and quadrature (Q—90 degree out of phase) signals into a composite single-sideband signal for transmission. Figure 6 demonstrates a baseband transmit architecture that performs an *analog* mix of the I and Q signal. In this example, two DACs are required per transmit channel. Even at the low output frequencies used in many baseband applications, the TxDAC family are the best choice because all family members combine (1) high SFDR at low output frequencies; (2) low power consumption, single supply and 3-V operation to enhance system power efficiency; (3) competitive pricing (overall cost can be further reduced by oversampling the signal (interpolation) to reduce the DACs' in-band aliased images, thus easing the job of the low-pass filter); and (4) the variety of resolutions offered in the same pin-out allows ultimate cost/performance trade-offs. For example, in many of the TxDAC beta-site applications, users started with one resolution model and later designed-in either a higher- or lower-resolution device based on actual system performance.

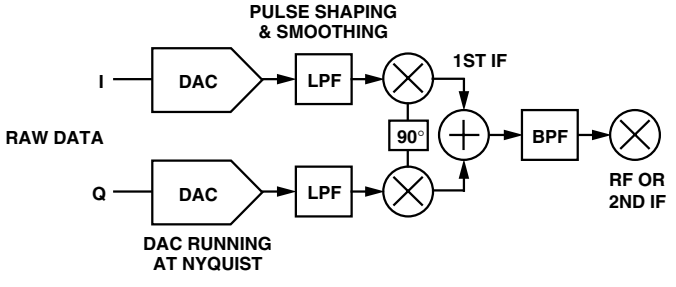



Figure 6. Baseband transmit architecture with analog quadrature mixing.

The system architecture in Figure 7 uses *digital* mixing of I and Q signals and inputs the modulated signal directly to a single DAC. In this case, the bandwidth requirements of the DAC are more stringent. With digital modulation, intermediate frequencies (IFs) in the range of 40 MHz can be generated via TxDAC chips. This is adequate for directly transmitting data in high-speed modems and upstream information in interactive set-top boxes. In other applications, it could eliminate an up-converter stage. Here, too, high SFDR, low price, low power, and family pin-compatibility are desirable (required) attributes. If multiple digital I&Q modulators were fed into the single DAC depicted in Figure 7, the system would correspond to a wideband transmit architecture, for which the superior multi-tone performance of the TxDAC family of products is a major performance attribute.

The 10-bit AD9760s are finding their way into high-speed Internet data modems and interactive set-top boxes where the SFDR requirements are in the 50 dB range, at 40 MHz output frequencies, clocking at rates of up to 120 MSPS. They are also being used in wireless local loop and high speed wireless trunking basestations. The 12-bit devices are being designed into cellular and personal communication service (PCS) basestations, cable head-end equipment, and hybrid fiber coax modems, where SFDRs of up to 70 dB are required at various clock and sample rates. The 14-bit AD9764 is finding a home in ADSL modems and next-generation PCS basestations where > 70 dB is desired for 1-MHz to 6-MHz signals at clock rates of < 15 MSPS.

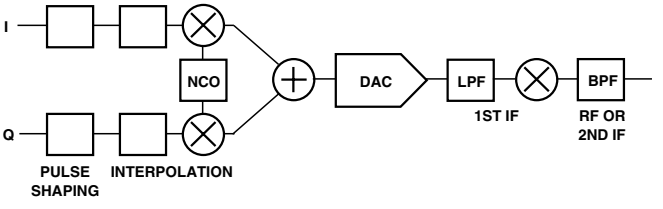



Figure 7. Transmit architecture with digital modulation.

A major benefit of chip design for plain-vanilla CMOS fabrication is digital integration compatibility. The TxDAC core, optimized on a *CMOS* process, enables efficient integration with digital-signal-processing (DSP) circuitry for additional board and cost savings, with enhanced performance capabilities and reliability. By integrating digital processing with the DAC core, higher-speed digital switching can be accomplished than ever before possible.

For example, in traditional two-chip direct digital synthesis (DDS) systems, using a digital DDS engine and a high-performance (bipolar) DAC, speed and resolution are limited by the speed and power required to clock the digital data out of the DDS chip into the DAC (TTL logic is limited to about 100 MSPS). By integrating the DDS circuitry with the DAC, internal data rates > 200 MSPS will be usable and economical. Besides single-chip high-performance DDS (see page 12), future on-chip digital circuitry will include digital modulators and interpolation filters.

The TxDAC family* products are packaged in 28-pin SOICs and are specified for –40 to +85°C. Evaluation boards are available. Prices (1000s) start at $7.84 for the AD9760AR-50, $12.54 for AD9760, $18.85 for AD9762, and $22.62 for AD9764. Evaluation boards for all models are priced at $150.

*The TxDACs were designed by Analog Devices Fellow Doug Mercer at our facility in Wilmington, MA.* A

*For technical data, consult our Web site, **http://www.analog.com, or circle 1**

# Buffered Multiplexers for Video Applications

by Eamon Nash

Video functions, such as scanners, video routers, and pixel-in-pixel switching are generating a need for high-speed switching with multiplexers (muxes) and crosspoint switches. Increasing system compactness demands switch ICs with low power consumption and increased functionality, such as the ability to drive 75-Ω or 150-Ω loads without additional buffering. They also require good video specifications, e.g., low differential gain and differential phase, good gain flatness, low crosstalk, and fast settling.

Figure 1 shows block diagrams of the AD8174 and AD8180, two members of a new family of buffered analog multiplexers (muxes), distinguished by excellent video specifications at high speeds and very low power consumption. The **AD8180** is a single 2-to-1 mux; the AD8182 (not shown) is a dual version. Both devices offer a –3-dB bandwidth of 750 MHz and a slew rate of 750 V/µs. With > 80 dB of crosstalk rejection and isolation at 5 MHz, they are useful in many high-speed applications. The differential gain and differential phase errors of 0.02% and 0.02°, plus 0.1-dB flatness to beyond 200 MHz, make them ideal for professional video muxing. Their 10-ns switching time makes them an excellent choice for pixel switching (picture-in-picture), while consuming less than 3.8 mA on ±5-V supplies.

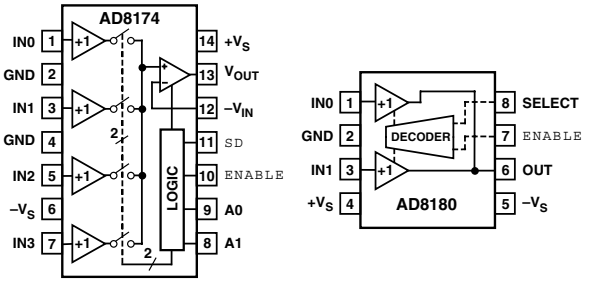



Figure 1. Block diagrams of the AD8174 and AD8180.

The **AD8174*** is a high-speed 4-to-1 multiplexer. Not shown is the AD8170*, a 2-to-1 mux with similar specs. These devices offer 200-MHz –3-dB signal bandwidth, slew rate greater than 1000 V/µs, and 0.1-dB gain flatness to 80 MHz. With a low 75 dB of crosstalk at 5 MHz, these devices are useful in many high speed applications.

The AD8170 and AD8174 contain a current-feedback output amplifier, whose gain can be programmed using external resistors. The amplifier has high output drive current of 50 mA and can drive a back-terminated 75-Ω load ($R_L$=150 Ω) to ±3.8 V. Power consumption is low at 8.25 mA (AD8170) and 9.7 mA (AD8174) from a ±5-V supply.

*Available November, 1996.

Self-contained buffering reduces power consumption, saves board space, and allows direct connection of muxes to high speed ADCs. This is especially important in the case of CMOS ADCs, which generally have variable input impedance, associated with switched capacitance.

## APPLICATIONS

**An 8 × 2 Crosspoint Switch:** While 8 × 8 and 16 × 16 crosspoint switches are commonly available, crosspoints with arbitrary numbers of inputs and outputs still must be designed using multiplexers as building blocks.

Figure 2 shows a modular 8 × 2 crosspoint switch that uses 4 AD8174 4-to-1 buffered muxes, two per 8-to-1 multiplexer channel. The $\overline{\text{Output Enable}}$ function on each device allows the outputs to be tied together. In this way, the $\overline{\text{Enable}}$ pin, with sense inverted to one of the multiplexers, can be used as the third address line on the 8-to-1 multiplexer.

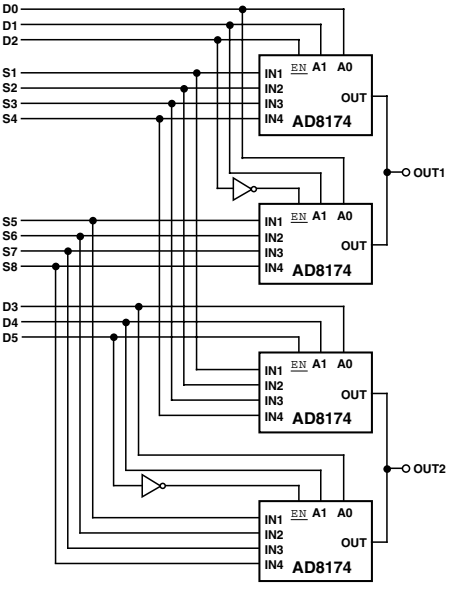



Figure 2. 8-input, 2-output crosspoint switch.

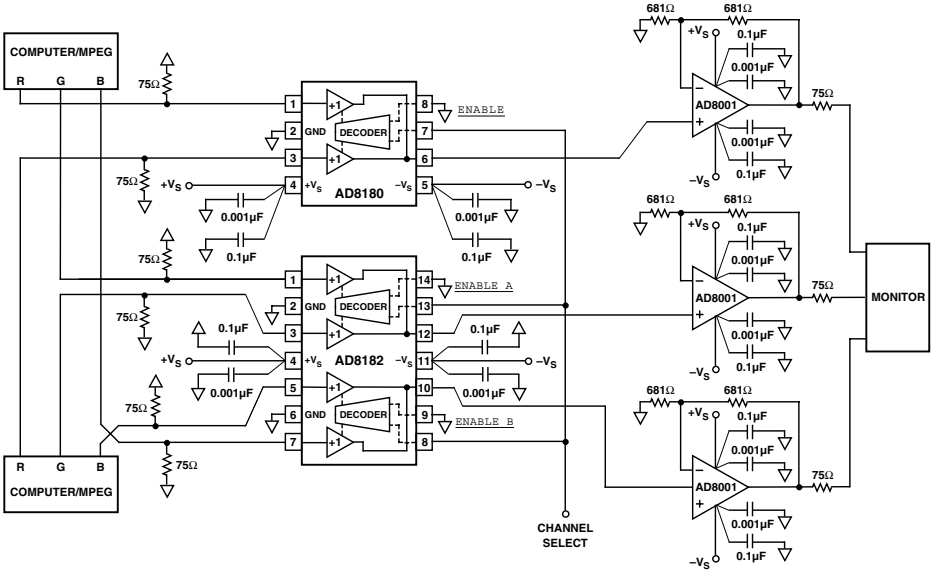



Figure 3. Switching two color video channels.

Connecting all eight input lines to both 8-to-1 multiplexers results in an 8 × 2 crosspoint switch. Any one of eight inputs can be switched to either of two outputs. The number of multiplexers that can be paralleled is limited only by the drive capability of the input signal sources. An input impedance of 2 MΩ and an input capacitance of 2 pF help to ameliorate this limitation. In applications where higher bandwidth is necessary, the AD8182 could be used to implement the same crosspoint function.

**Multiplexing two Video Sources:** A common video application requires two RGB sources to be multiplexed together before the selected signal is applied to a monitor (e.g., a PC's normal output and a specialized source, such as MPEG video). Figure 3 shows how such a circuit could be realized using the AD8180 and AD8182.

Because all three multiplexers are permanently active, the $\overline{\text{ENABLE}}$ pins are tied permanently low. The three SELECT pins are tied together and this signal is used to select the source. In order to drive a 75-Ω back-terminated load ($R_L$ = 150 Ω) and provide an overall gain of unity, the multiplexer outputs are buffered using AD8001 current-feedback op amps configured for gain of 2.

**Picture-in-Picture or Pixel Switching:** Many high-end display systems require simultaneous display of two video pictures on one screen. Video conferencing is one such example. The remote site might be displayed as the main picture with a picture of the local site "inset" for monitoring purposes. The circuit of Figure 3 could be used to implement this "picture-in-picture" application.

Implementing a picture-in-picture algorithm is difficult. Both sources are being displayed simultaneously (i.e., during the same frame) and both sources are in real time. Figure 4 shows the raster-scanning common to all monitors. During each horizontal scan that includes the inset, the source must be switched twice (i.e., from main to inset and from inset to main). To avoid screen artifacts, switching must be clean and fast. The AD8180, used in the above application, switches and settles to 0.1% in 10 ns. Root-square-summed with the 10-ns settling time of the AD8001, the overall settling time is 14 ns. This yields a sharp, artifact-free border between the inset and the main picture.

The video source selector of Figure 3 could also be implemented with three AD8170 buffered multiplexers. Since this device has high output drive current and is capable of delivering ±3.8 V into a 150-Ω load, it doesn't require an external high current buffer op amp. In addition, the inverting input of the output buffer is pinned out so that a closed loop gain of 2 can be set.

In Figure 5, the video signals from two current output RAM-DACs are multiplexed using the AD8170. The selected signal drives a monitor. RAM-DACs typically deliver a full scale current of 26.67 mA. A doubly terminated 75-Ω line presents an effective resistance of 37.5 Ω to the DAC and converts the current into a full-scale voltage of 1 V (100 IRE or video white level) at the input to the multiplexer. Doubly terminating is good practice, minimizing

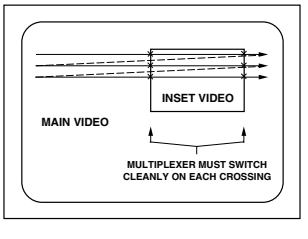



Figure 4. The key to clean picture-in-picture switching.

reflections, because the load and source impedances are both equal to the characteristic impedance of the line. Because the RAM-DAC has a relatively high output impedance, the source resistance is close to 75 Ω.

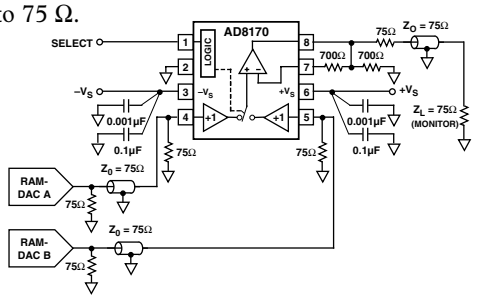



Figure 5. Complete switching for two video sources.

The output of the multiplexer must drive a back-terminated line. In order not to lose signal level, it is necessary to double the signal amplitude before application to the line. This can be conveniently done by setting the gain of the multiplexer's output op amp to +2.

**Color Image Scanner:** Charge-coupled devices (CCDs) find widespread use in scanner applications. A monochrome CCD delivers a serial stream of voltage levels; each level is proportional to the light shining on a single cell of the CCD. For the color image scanner shown in Figure 6, there are three output streams, representing red, green and blue. Interlaced with the stream of voltage levels is a voltage representing the reset level. A correlated double sampler (CDS) subtracts these two voltages from each other.

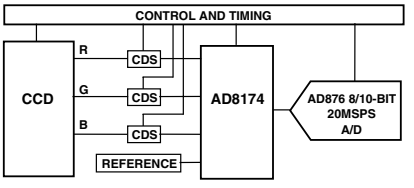



Figure 6. Color image scanning.

The next step in the data acquisition process is to digitize the three signal streams. Assuming that the ADC chosen has a fast-enough sample rate, multiplexing the three streams into a single ADC is more economic than using three ADCs. Here, the AD8174 multiplexes the red, green and blue channels into the AD876, an 8- or 10-bit 20-MSPS ADC. Because of its wide bandwidth, the AD8174 can drive the AD876's switched-capacitor input stage without additional buffering. In addition to the bandwidth, it is necessary to consider the settling time of the multiplexer. The ADC's 20-MHz sample rate corresponds to a sampling period of 50 ns. Typically, one phase of the sampling clock is used for conversion, with all levels held steady; the other phase is used for switching and settling to the next channel. For a 50% duty cycle, the signal chain must settle within 25 ns. The 18-ns mux settling time to 0.1% easily satisfies this criterion.

The fourth (spare) channel of the AD8174 is used to occasionally measure a reference voltage. Muxing a reference voltage offers the advantage that any temperature drift effects caused by the multiplexer will equally impact the reference voltage and the CCD signals. If the fourth channel is unused, it is good design practice to tie it permanently to ground.

*The AD81xx multiplexer family was designed by Kimo Tam, in Wilmington, MA, and JoAnn Close, in Santa Clara, CA.* A

For technical data, consult our Web site (www.analog.com) or **Circle 2**

# Single-Chip Direct Digital Synthesis vs. the Analog PLL

## Complete-DDS chips with DAC have excellent AC performance, low power & price, small size

by Jim Surber and Leo McHugh

New integrated Complete-DDS products present an attractive alternative to analog PLLs for agile frequency synthesis applications. Direct digital synthesis (DDS) has long been recognized as a superior technology for generating highly accurate, and frequency-agile (rapidly changeable frequency over a wide range), low-distortion output waveforms. DDS architecture (Figure 1) employs a precision phase accumulator and digital signal-processing techniques to generate a digital sine wave representation which is referenced to a highly-stable reference clock. The digital sine-wave data is then applied to a high-speed D/A converter (DAC) to generate a corresponding analog sinewave output signal.

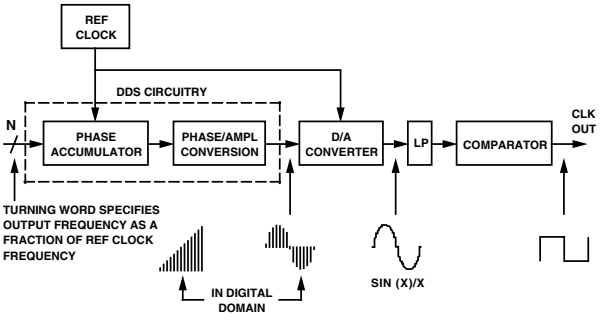



Figure 1. Basic Complete-DDS system block diagram.

A major advantage of a DDS system is that its output frequency and phase can be precisely and rapidly manipulated under digital processor control. Other inherent DDS attributes include the ability to tune with extremely fine frequency- and phase resolution (frequency control in the millihertz (mHz) range and phase control < 0.09°, and to rapidly "hop" in frequency (up to 23 million output frequency changes per second). These characteristics have combined to make the technology extremely popular in military radar and communications systems. In fact, DDS technology was previously relegated almost exclusively to high-end and military applications: it was costly, power-hungry (dissipations specified in *watts*), difficult to implement, required a discrete high-speed signal DAC, and had a set of user-hostile system interface requirements.

A new family of breakthrough CMOS digital synthesizer products from Analog Devices increases the attractiveness of DDS-based synthesizer solutions. The AD9850 and AD9830125-MHz and 50 MHz *Complete-DDS* (C–DDS) devices include on-chip 10-bit signal DACs (Figures 2 and 3). They are optimized for low output distortion, with spurious-free dynamic range (SFDR) of 72 dBc narrowband and up to 54 dBC wideband @ 40 MHz. Additional product features, such as small surface-mount packaging, extremely low power dissipation (as low as 155 mW at +3.3 V), increased functionality, and low price, combine to ensure that these devices are indeed the State-of-the Art in DDS technology. They now permit users to address cost-sensitive, high-volume, consumer synthesizer applications; and they present a viable alternative to analog-based phase-locked loop (PLL) technology for generating agile analog output frequency.

The AD98x0 devices should be uniquely attractive for local oscillator (LO) and up/down frequency conversion stages—which were until now the exclusive domain of PLL-based analog synthesizers. The Complete-DDS architecture of the AD98x0 devices holds distinct advantages over an equivalent PLL-based agile analog synthesizer for many reasons. For example:

- **Output frequency resolution**: the AD98x0 C-DDS products have 32-bit phase accumulators, which enable output frequency tuning resolutions much finer than a PLL-based synthesizer can enjoy. The AD9850 has a tunable output resolution of 0.06 Hz, with a clock frequency of 125 MHz; the AD9830 has a tuning resolution of 0.012 Hz, with a reference clock of 50 MHz. Furthermore, the output of these devices is phase-continuous during the transition to the new frequency. In contrast, the basic PLL-based analog synthesizer typically has an output tuning resolution of *1 kilohertz*; it lacks the inherent resolution afforded by the digital signal processing.
- **Output-frequency switching time**: the analog PLL frequency switching time is a function of its feedback loop settling time and VCO response time, typically > 1 ms. C-DDS-based synthesizer switching time is limited only by DDS digital

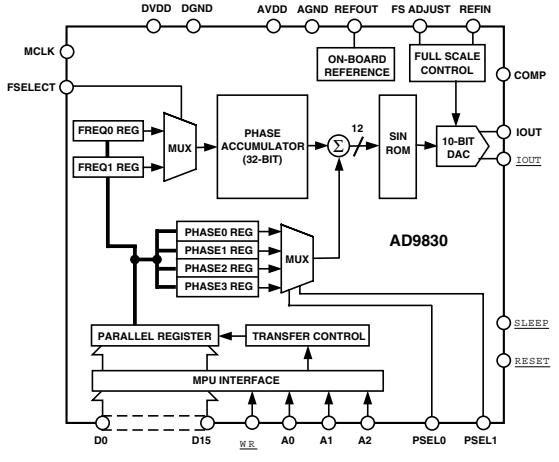



Figure 2. Block diagram of AD9830 50-MHz C-DDS.

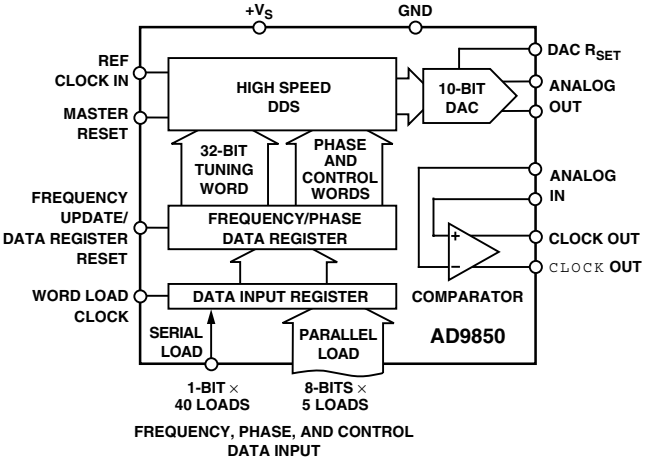



Figure 3. Block diagram of AD9850 125 MHz C-DDS.

processing delay; the AD9850's minimum output frequency switching time is 43 ns.

- **Tuning range:** A critical feedback loop bandwidth and input reference frequency relationship determines the stable (usable) frequency range of the typical analog PLL circuit. C-DDS-based synthesizers are immune to such loop filter stability issues and are tunable over the full Nyquist range (< 1/2 the clock rate).
- **Phase noise:** Because of the frequency division, C-DDS-based solutions have a clear advantage over analog PLL synthesizers in output phase-noise. The output phase noise of a C-DDS synthesizer is actually better than that of its reference clock source, while analog PLL-based synthesizers have the disadvantage of actually multiplying the phase noise present in their frequency reference.
- **Board-space requirement:** The highly integrated AD98x0 C-DDS devices are packaged in very small surface-mount packages requiring no more board space than most high-quality equivalent-bandwidth discrete PLL synthesizer implementations.
- **Cost:** Shattering existing DDS price barriers, C-DDS-based solutions are competitive in high-volume applications with bandwidth-equivalent discrete PLL-based synthesizer solutions.
- **Power-dissipation:** C-DDS synthesizers dissipate much less power than earlier discrete DDS solutions. For example, the AD9850 dissipates 155 mW at 3.3 V when generating a 40-MHz signal, with a 100 MHz reference clock. This is competitive with comparable discrete analog PLL circuits.
- **Implementation complexity:** Complete-DDS solutions, which include the signal DAC, translate to ease of system design. There is no longer an element of RF design expertise required to implement a DDS solution; the hard part has been done. A simple digital instruction set for control minimizes the complexity of support hardware. Digital system design replaces the analog-intensive system design required for PLL-based analog synthesizer solutions to similar problems.

AC performance is an important consideration in the choice of a frequency synthesizer. The distortion performance of a C-DDS synthesizer system is limited by its signal DAC; and the AD98x0 devices set a new benchmark in CMOS DAC performance. Their

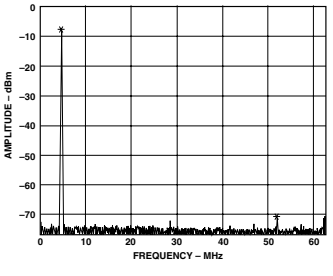



Figure 4. AD9850 wideband spectral plot at 5 MHz Aout (125-MHz clock).

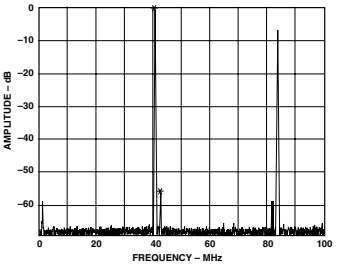



Figure 5. AD9850 wideband spectral plot at 40 MHz Aout (125-MHz clock).

on-board 10-bit DAC cores have been intensively optimized for high SFDR over wide output bandwidths, and are technological breakthroughs in their own right (see pages 7-9 of this issue). Figures 4 and 5 show wideband spectral plots of the output of the AD9850 generating 5-MHz and 40-MHz output frequencies with a 125-MHz reference clock. The demonstrated SFDR of the output of the AD9850 is 62.8 dB and 55.2 dB (respectively) over the 62.5 MHz Nyquist bandwidth (1/2 the reference clock rate). Such dynamic performance was previously achievable only with expensive bipolar DACs dissipating several watts.

In other applications, many of them dominated by analog PLL-based synthesizer solutions, *narrowband* performance is an important consideration. In narrowband applications the spur performance of the C-DDS synthesizer's output is largely gated by the digital truncation level of the DDS rather than DAC's performance. Figure 6 shows a narrowband plot of the AD9830 at 4.16-MHz $A_{out}$ and a 50-MHz clock. The SFDR is shown to be greater than 79 dB over a ±5 kHz window of the fundamental.

Both the AD9850 and the AD9830 utilize a very simple loading

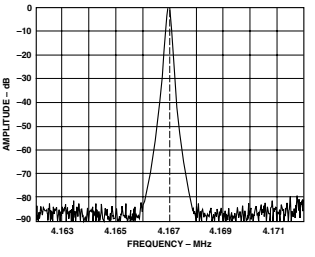



Figure 6. AD9830 narrowband spectral plot at 4.1 MHz Aout (50 MHz clock).

scheme for user-friendly operation. They require only a data clock and data/address bus to control the output frequency and phase and to enable the sleep mode. No analog-intensive system design is required, except for the specific requirements of output filtering. The AD9850 has a useful additional feature: an integrated high-speed comparator. The filtered output of the DAC can be applied to this comparator to generate a square wave out instead of a sinewave, facilitating the use of the device as a frequency-agile clock generator. PC-compatible evaluation boards are available for both devices to facilitate bench testing of the synthesis system.

The combination of fast output hopping, digital control, low output distortion, and high tuning resolution makes the Complete-DDS solution a viable alternative to analog PLL synthesizers. The AD9830 and AD9850 breakthroughs in CMOS DAC and DDS technology warrant serious consideration for any frequency synthesizer requirement.

*The AD9830 was designed in Limerick, Ireland, by Hans Tucholski, and the AD9850 was designed i n Greensboro, NC, by Dave Crook and Tim Stroud* A

| **Feature/Specification** | **AD9850** | **AD9830** |
|---|---|---|
| Maximum clock frequency | 125 MHz | 50 MHz |
| Maximum output Nyquist-frequency bandwidth | 62.5 MHz | 25 MHz |
| Frequency tuning word resolution | 32 bits | 32 bits |
| Phase tuning word resolution | 5 bits | 12 bits |
| Supply voltage | +3.3 V or +5 V | +5 V |
| Power dissipation @ max. operating conditions | 155/380 mW | 265 mW |
| Worst-case narrowband SFDR (±50-kHz window) @ max. clock | 72 dBc | 72 dBc |
| Wideband SFDR (Nyquist) @ 20-MHz $A_{out}$ | 58 dBc | 50 dBc |
| Wideband SFDR (Nyquist) @ 40-MHz $A_{out}$ | 54 dBc | N/A |
| Control interface | Parallel/serial | Parallel |
| Unique additional features | Internal high-speed comparator registers | Two frequency four phase registers |
| Package style | 28-pin SSOP | 48-pin TQFP |
| Price (100s) | $14.55 | $11.70 |
| Faxcode* | 1990 | 1993 |

*Technical data is available at our World Wide Web site (www.analog.com); via AnalogFax™ (1-800-446-6212]; or the reply card, **Circle 3**

# For Efficient Signal Processing in Embedded Systems, Take a DSP, not a RISC

by Jerry McGuire

Increasingly, electronic equipment applications involve signal processing. Home theatre, computer graphics, medical imaging and telecommunications all rely on signal-processing technology. Signal processing requires fast math in complex, but repetitive algorithms. And many applications require computations in real-time: i.e., the signal is a continuous function of time, which must be sampled and converted to digital, for numerical processing. The processor must thus execute algorithms performing discrete computations on the samples as they arrive.

The architecture of a digital signal processor (DSP) is optimized to handle such algorithms. The characteristics of a good signal processing engine include: fast, flexible arithmetic computation units (e.g., multipliers, accumulators, barrel shifters); unconstrained data flow to and from the computation units; extended precision and dynamic range in the computation units (to avoid overflow and minimize roundoff errors); dual address generators (for simultaneous handling of both inputs to a dyadic operation); efficient program sequencing (including ability to deal with loops and interrupts effectively); and ease of programming.

A DSP has some of these features in common with a reduced-instruction-set-computer (RISC). In addition, both are constructed around certain core instructions, enabling them to operate at very high instruction rates; and both eschew internal microcode. However, they are fundamentally different "animals". The differences between RISCs and DSPs are most pronounced in the processors'

- computational units
- data address generators
- memory architectures
- interrupt capabilities
- looping hardware
- conditional instructions
- interface features

DSPs belong to two basic classes: *fixed point*, a (typically) 16-bit architecture based on 16 bit integer data types, and *floating point*, usually with a 32-bit architecture, based on a data type that has both mantissa and exponent.

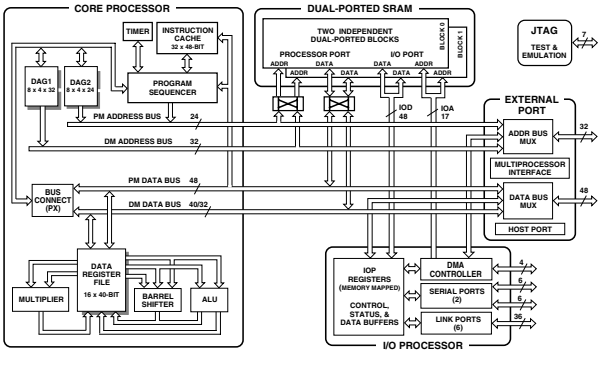



Figure 1. SHARC internal architecture.

**Computational Units:** DSPs all contain parallel hardware *multipliers* to support single-cycle multiplication, and their multipliers often combine multiplication and accumulation in a single cycle. DSPs have dedicated *accumulators* with registers significantly wider than the nominal word size to preserve precision—for example, 80 bits in the 32-bit ADSP-2106x SHARC family (Figure 1). Hardware may support recovery from accumulator overflows, as with the ADSP-21xx family. In addition, DSPs all contain full-featured *arithmetic-logic units* (ALUs), independent of the multiplier.

The ALU may have special features, such as the ability to produce simultaneous sums and differences to accelerate the kernel routine in the fast Fourier transform (FFT)—an algorithm for transforming signals between the time domain and the frequency domain. An advanced DSP will contain saturation logic in the computational units to prevent data overflow. It also may offer zero-overhead (i.e., without requiring additional clock cycles) traps to interrupt routines on arithmetic exceptions.

A sophisticated DSP may also contain a single-cycle *barrel shifter* (i.e., one capable of shifting a word an arbitrary number of bits left or right in one clock cycle), with a priority encoder for data scaling, data compression/expansion or packing/unpacking and bit manipulation. It may also include dedicated hardware to minimize the time required for fast division, square root, and transcendental-function calculation. Computational elements with these specialized features are not found on RISC processors.

**Address Generation:** An efficient DSP will keep its computational units fed with data from at least two independent *data-address generators*. Tapped delay lines and coefficient buffers are characteristic of DSPs, yet are mostly unknown in general-purpose computing. An efficient DSP needs circular-buffer hardware to support the buffers. Circular buffer pointers need to be updated every cycle without overhead. Furthermore, a comparison test for end-of-buffer needs a no-delay command to reset the pointer at the end-of-buffer. On the other hand, a RISC processor requires an additional cycle for each comparison test.

**Memory Architectures:** DSPs typically support system memory architectures that differ from those in general-purpose computing systems. DSPs utilize a *Harvard architecture*, which permits sustained single-cycle access to two words of data from two distinct external memories. Analog Devices SHARC DSPs, for example, feature 2 or 4-Mbits of dual-ported SRAM integrated on-chip. This memory is directly addressed—not a cache, as would be found in RISC processors. To the CPU, this on-chip memory looks like a unique piece of memory, not merely a high-speed replica of memory elsewhere in the system. The reason is that DSPs are typically embedded processors. Their on-chip memory is often adequate to contain the complete, repetitive DSP program necessary to the task. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller (Figure 2). The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

**Interrupt capabilities:** Because DSPs are intended for operation in real-time systems, efficient, sophisticated, and predictable interrupt handling is critical to a DSP. RISC processors, with their highly-pipelined architectures, tend to have slow interrupt response

times and limited interrupt capabilities. Context switches should be very fast. Advanced DSPs, like the new ADSP-21csp01 and Analog Devices' ADSP-2106x floating-point family support *complete sets of alternative registers*, allowing a single-cycle switch of context to support interrupt handling. (Register-file windowing differs, in that its purpose is to accelerate parameter passing, not save an entire context.)

An advanced DSP will support at least four independent external interrupts in addition to internal interrupts. Interrupt latency will be kept to just a few cycles and must be predictable. Interrupts should be nestable and prioritizable. In addition, it should be easy to enable and disable particular interrupts in real time.

**Hardware looping:** Efficient *looping* is critical to digital signal processing because signal-processing algorithms are repetitive. A good DSP will support zero-overhead loops with dedicated internal hardware. That is, the chip will monitor loop conditions and terminations to decide-in parallel with all other operations-whether to increment the program counter or branch without cycle-time penalty to the top of the loop. A RISC processor, on the other hand, has to do a test-and-branch at the end of every loop, costing at least an additional cycle every loop and every pass. Nested loops are also very common in signal processing algorithms; the DSP looping hardware should support a depth of at least four levels of nested loops. RISC processors have yet to evolve to support these basic signal processing needs.

**Conditional execution:** Data-dependent execution is important for signal processing. For this reason, advanced DSPs, like the ADSP-2100 family and the ADSP-2106x SHARC floating-point family, support *conditional execution* of most of their basic instructions: in a single instruction, the processor tests a condition code and, if true, performs an operation in the same cycle. This can make an enormous difference to computationally intensive algorithms. Intel discovered this problem with the i860 and added a graphics unit to handle the conditional store operations necessary for high-performance Z-buffering.

**Interfaces:** DSPs operate on real-world signals coming from analog-to-digital converters, and they send their results to D/A converters. For this reason, DSPs often contain serial ports for an inexpensive interface to these devices. Advanced DSPs add hardware to make the operation efficient, for example, double-buffering and auto-buffering. Because these input/output signals may come from and go to nonlinear codecs, an advanced DSP may have dedicated hardware for zero-overhead *A*-law and $\mu$-law companding. In addition, the serial ports may have features to simplify interfacing with T1 and CEPT data transmission lines.

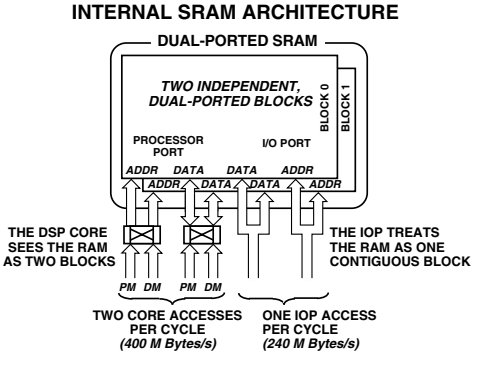



Figure 2. The efficient SHARC memory architecture allows I/O bandwidth to keep up with computations.

The SHARC serial ports are designed to maximize throughput with hardware that is flexible, yet tuned to various signal types. Their features include: each serial port can automatically receive and/or transmit an entire block of data, independently transmit and receive—each with a data buffer register as well as a shift register, multi-channel mode for TDM.

**Programming considerations:** At one time, a significant difference between DSPs and RISCs was their programming models. DSP is inherently performance-driven, so programming of DSPs was done mostly in assembly language to get the best performance from the processor. This is generally still true for fixed-point DSPs, but much more easily so with the ADSP-2100 family's intuitive algebraic assembly language (Figure 3). At no sacrifice to performance, it ameliorates the ease-of-use issue that drives many programmers to favor high-level languages like C.

```
f11=f1*f7, f3=f9+f14, f9=f9-f14, dm(i2, m0)=f13, f7=pm(i*, m8);
```

**In a single 25ns cycle, the ADSP-2106x performs:**
- **1 Multiply**
- **1 Addition**
- **1 Subtraction**
- **1 Memory Read**
- **1 Memory Write**
- **2 Address Pointer Updates**

**While its I/O processor performs:**
- **Active Serial Port Channels (2 Transmit, 2 Receive)**
- **Active Link Ports (6)**
- **Memory DMA**
- **2 DMA Pointer Updates**

Figure 3. FFT code example.

On the other hand, floating-point DSPs are more efficiently programmed in high-level language. Floating-point calculations avoid fractional data types, which do not exist in C. In addition, architectural decisions can affect compiler efficiency. The large, unified address space of the ADSP-2106x SHARC family, for example, makes memory allocation easier for the compiler. In addition, their large, flexible register file improves efficiency.

Central to our product strategy is providing the tools and DSP cores that make it possible to efficiently program our fixed- and floating-point DSPs in high-level language. This is the driving force behind the ADSP-21csp, a new family of concurrent signal processors. Nevertheless, though using high-level languages, a DSP programmer must be able to descend in language level (with minimal pain) to improve performance of time-critical routines.

Increasingly, DSP designs are programmed in this sequence: first, a software prototype is written and debugged in a high-level language. This prototype often results in adequate performance. More generally however, increased performance will be required, so the high-level code is histogrammed in simulations to find the sections needing the most execution time. The critical sections are then hand-coded in assembly language. The histogramming and hand-coding process is iterated until performance targets are met.

While the differences between DSPs and RISCs are many, the two architectures tend to converge in the area of programming, a convergence driven by time-to-market and the evolving role of DSP in applications. Programmers, skilled at quickly developing working C programs, use them to bring product to market faster. Meanwhile, DSPs take on more system-management functions, such as the user interface or system control, and will need to offer high-level language efficiency to compete with the $\mu$Cs and RISC processors formerly assigned these control tasks. A

# New Product Briefs (For information use reply card or see back cover)

## Amplifiers and Preamplifiers

## Mike Preamplifiers

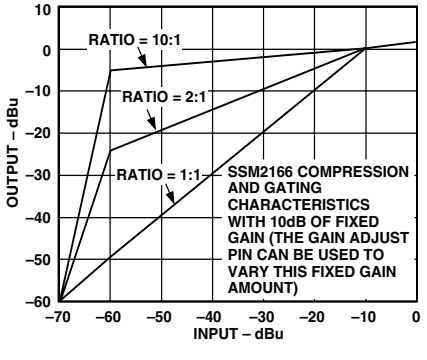
### Variable compression and noise gating: SSM2165/66

The SSM2165 and SSM2166 are complete microphone signal-conditioning "systems on a chip." A low-noise voltage-controlled amplifier (VCA) provides essentially distortionless gain that is dynamically adjusted by a control loop to maintain preset compression characteristics.

Gain is low at high input amplitudes (for limiting) and increases as input decreases (to reduce the output dynamic range). For example, with 10 dB of gain and a 10:1 compression ratio (see figure), a –60-dBu input amplitude (1 mV) will be amplified up to –5 dBu (435 mV), while a –10-dBu input (245 mV) will be amplified to 0 dBu (775 mV). A single resistor sets compression ratio (1:1 to 15:1). A "noise gate" downward expander reduces noise.

The compression will provide a steady output, little affected by voice levels and distance from the speaker to the microphone. Principal applications are to provide signal limiting without distortion, reduce background noise, and improve the intel-ligibility of voice signals for computer sound, teleconferencing, surveillance, etc.

Both devices provide a similar function. The flexible **SSM2166**, with adjustable gain from 0 to +20 dB, is available in 14-pin plastic DIP and narrow SOICs, while the simpler **SSM2165**, available in two fixed-gain versions (+10 and +20 dB), is housed in compact 8-lead DIPS and SOICs. Both are designed to operate on +5-V single supply over the –40 to +85°C temperature range. Prices start at $1.20 in 10,000s. **Circle 4** A



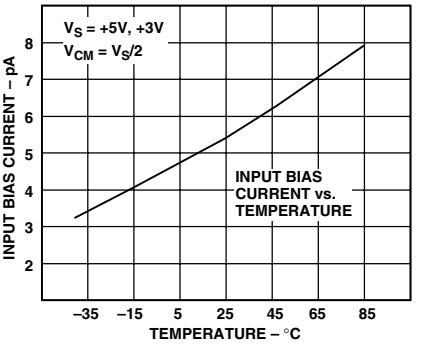

## Low-Cost 250-mA Rail-to-Rail Op Amps

### Single-supply AD8532 (dual), AD8534 (quad) Specified for operation with +3-V and +5-V supplies

The AD8532 and AD8534 dual and quad CMOS op amps feature excellent current specifications in all departments: high drive current (±250-mA typical—resistive & capacitive loads); low bias current (60 pA max over temperature—probes and integrators), and low quiescent current (1 mA max per amplifier with 3-V supply—3 mW/channel).

The output can swing essentially rail-to-rail (to within 100 mV), and the input common-mode range is equal to the supply voltage. AC performance is very good, with 3-MHz bandwidth, 5-V/µs slew rate, low distortion, and unity-gain-stable dynamics. Applications include audio amplification for computers, sound ports, sound cards, and set-top boxes, buffering of CMOS DACs, and as a drive amplifier for LCD panels.

All devices are specified over the extended industrial (–40 to +85°C) range. The




AD8532 is available in 8-lead SO and epoxy DIP, and the AD8534 is available in 14-lead DIP and narrow-body SO,. and TSSOP; and the AD8534 is available in 14-lead SO, epoxy DIP, and TSSOP (2500-piece reels). Respective prices (1000s) for AD8532 and AD8534 (SO and DIP) are $0.92 (92¢) and $1.42 (<36¢ per channel). **Faxcode* 1980** A

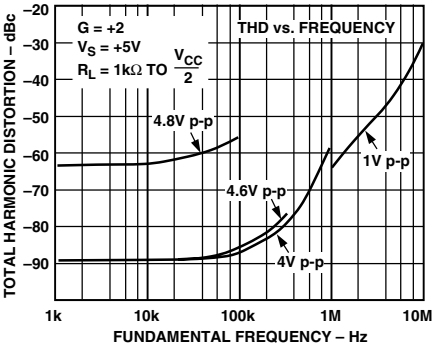
## 80-MHz Rail-to-Rail Voltage-Feedback

### AD8031 and dual AD8032 op amps are specified for +2.7 V and +5 V (800 µA typ/amp) single supply and ±5 V

The AD8031 and AD8032 voltage-feedback amplifiers feature high-speed performance, with 80-MHz small-signal bandwidth, 30-V/µs slew rate, and 125-ns settling time to 0.1%. Such performance is achieved while consuming 4 mW from a single +5-volt supply, which should lead to extended operation time in high-speed battery-powered systems.

These amplifiers have rail-to-rail input and output capability: Inputs can swing to 500 mV beyond each rail, and the output can swing to within 20 mV of the rails, providing wide dynamic range. They are characterized by low distortion: –62 dBc THD with a 2-V p-p, 1-MHz output signal, and –86 dBc for 100-kHz, 4.6-V p-p, on a +5-V supply (see illustration).

The AD8031/32 can operate on 2.7 to 12 V single supplies, up to ±6 V dual. They are ideal for applications in battery-operated systems needing wide bandwidth, as well as




high-speed systems with high component density requiring lower power dissipation. A premium dc 'B' grade is available for high gain applications with 1.5-mV max offset.

They are available in 8-pin plastic DIP and SOIC packages and will operate over the industrial temperature range of –40 to +85°C. Prices start at $1.45 (AD8031A in 1000s). **Faxcode* 1983** A



*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

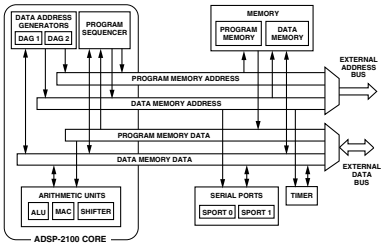
# DSPs and Digital & Analog Audio

## Low Cost DSP μC with on-Chip Memory

### ADSP-2104 and ADSP-2109 combine fast signal Processing and low-cost tools with low unit price

With the new ADSP-2104 ultra-low-cost DSP microcomputer, designers no longer must compromise performance for low cost. The ADSP-2104 integrates SRAM, peripherals, and our widely supported "2100" 16-bit fixed-point DSP core into a single chip, allowing the design of ultra-low-cost DSP systems using just three chips: the DSP, an EPROM, and a codec. For further savings, the external EPROM chip can be eliminated using the ADSP-2109, which has 4K of customer-defined, factory-programmed on-chip ROM.

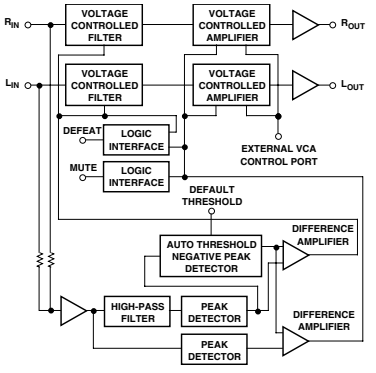
The signal-processing speed and level of integration of the new devices targets price-sensitive applications, such as radar detectors, dictation machines, telephone-answering machines, speakerphones, asynchronous motors, power meters, music synthesizers, and toys.




The ADSP-2104 integrates 256 words of SRAM for data memory and 512 words for program memory. Each device is available in a 68-lead PLCC, for operation from 0 to +70°C. The ADSP-2104 is supported by the EZ-KIT Lite Developer's Kit and 2100-family development tools. The devices operate on +5-V supplies, and 3.3-V "L" versions are available where power consumption must be minimized. Prices start at $5.25 in 10,000s. EZ-KIT Lite is only $89. **Circle 5** A

## Noise-Reduction IC

### SSM2000: Noise reduced 25 dB. No pre-encoding!




The SSM2000 (*Analog Dialogue* 30-2, 1996, p. 10) is an audio dual-channel noise-reduction IC. It reduces noise by combining variable filtering and downward expansion, in conjunction with a unique adaptive noise-threshold detector.

Pre-encoding of program material is not required; yet these techniques combine to yield an overall noise reduction of up to 25 dB on a variety of program sources: AM and FM radio, open-reel and cassette tape, LPs, CDs, Dolby-B®-encoded programming, broadcast studio-transmitter links and telephone lines, etc.—without the need for any manual adjustment.

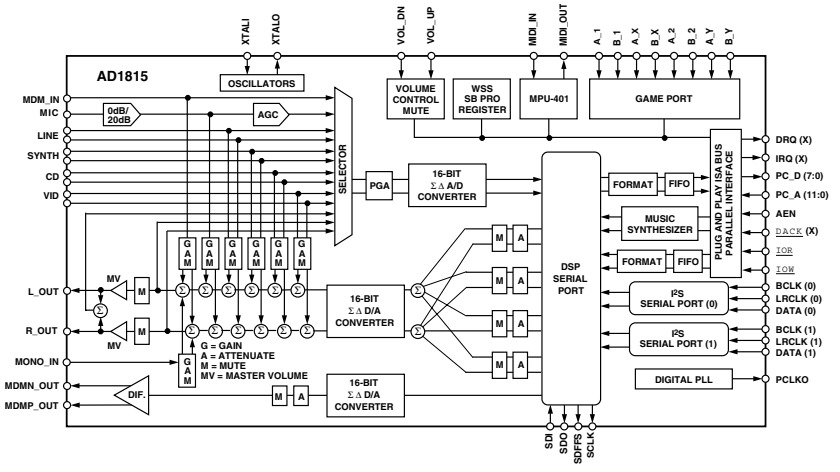
The HUSH® Noise Reduction System (HUSH is a registered trademark of Rocktron Corporation), as implemented in the SSM2000, has been demonstrated to reduce noise substantially—while preserving fidelity and transparency—in PC multimedia, intercom systems, teleconferencing systems, mobile communications, automotive audio, home stereos and TVs, and other consumer and professional audio applications.

With a few added components, and using its accessible VCA port, the SSM2000 becomes an automatic sound-level management system, which maintains comfortable volume levels despite changes in signal level and/or external noise. The SSM2000 is available in 24-lead plastic DIP and SOIC for the –40 to +85°C temperature range. Prices start at $6 in 100s. **Faxcode* 1952** A

## SoundComm Single-Chip Plug and Play

### AD1815 Controller supports applications written for SoundBlaster Pro™, Adlib/OPL3™, Win 3.1, Win 95

The AD1815 SoundComm™ Controller is a single-chip Plug and Play audio system for adding 16-bit stereo audio and communications support to personal computers. It provides an integrated audio solution for Windows 95, Windows 3.1, DirectSound, and multimedia applications. It supports telephony with a V.34-compatible modem analog front end and a serial port linking it to a companion media pump or DSP. It is packaged in a 100-lead PQFP. Prices start at $17.50 in 1000s. **Circle 6 A**

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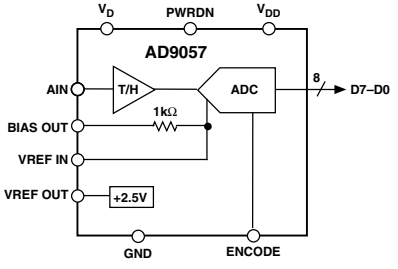
# ADCs and Direct Digital Synthesis

## 8-bit, 60-MSPS ADC

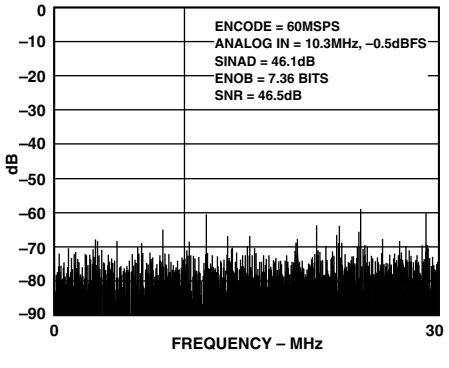
### Lo-power AD9057:200 mW < 10 mW in power down




The AD9057 is an 8-bit monolithic sampling A/D converter, with a 1-V p-p input range, optimized for low cost, low power, small size, and ease of use. With a 60-MSPS encode-rate capability and full-power analog bandwidth of 120 MHz, it will serve well in applications requiring excellent dynamic performance. It is a complete conversion solution with internal 2.5-V reference, requiring only a +5-V supply and encode clock.

It's encode input is TTL/CMOS compatible, and the 8-bit parallel digital outputs can be operated from +5 or +3-V supplies. In powerdown, the digital outputs go to high impedance, and total power consumption is less than 10 mW. Typical applications include digital communications (QAM demodulators), composite video processing, read channels, medical imaging, and digital instrumentation.

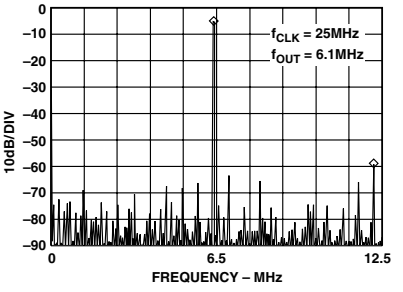
Housed in a 20-pin SSOP, its operating temperature range is –40 to +85°C. An evaluation board is available. Prices start at $7.28 in 1000s. **Faxcode* 2007** A




## Low-Power 25-MHz Complete-DDS

### 3-V/5-V AD9831 10-bit direct digital synthesizer Includes output DAC, Power-down mode, 70-dB SFDR

The AD9831, like the AD9830 (page 12), is a monolithic complete-DDS (C-DDS) CMOS chip—a numerically controlled oscillator comprising a phase accumulator, a sine lookup table, and a 10-bit D/A converter with 4-mA full-scale output. It supports clock rates up to 25 MHz and provides capabilities for phase- and frequency modulation. Applications include digital demodulation and tuned direct digital synthesis.




Frequency accuracy can be controlled to 2.5 parts in $10^{10}$. Modulation is effected by loading registers through the parallel microprocessor interface. With a 25-MHz clock, and generating a 1.055-MHz sine wave, performance includes 50 dB min SNR, –55-dBc total harmonic distortion, and 70 dB/55 dB narrowband/wideband min spurious-free dynamic range (SFDR).

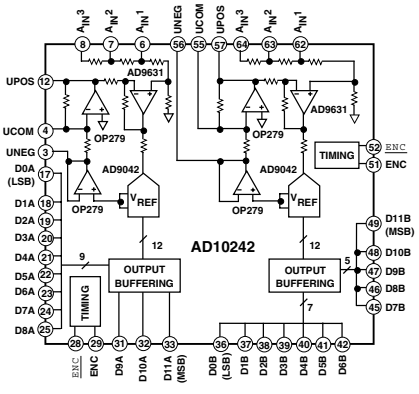
The device has an internal 1.21-volt reference, which is available externally. The AD9831 consumes 150 mW with 5-V supply and 35 mW at 3 V. A power-down pin allows external control of a power-down mode (< 10 mW). The device is housed in a 48-pin TQFP, and operation is from –40 to +85°C. Prices start at $6.25 in 1000s. **Faxcode* 1994** A

## Dual 12-Bit, 40-MSPS ADC

### AD10242 has matched data-acquisition channels, ±0.5-V, ±1.0-V, ±2.0-V inputs; uses ±5-V supplies

The AD10242 is a complete 12-bit dual data-acquisition system MCM in a 68-lead ceramic leaded chip carrier. It combines two sets of high-performance chips, including input amplifiers, references, and *a pair of AD9042 ADCs*, with output buffers having separate parallel data connections. Each channel is laser-trimmed for gain and offset matching, and provides channel-to-channel crosstalk < 80 dB.

Near Nyquist, with a 19.5-MHz input signal, signal-to-noise ratio (SNR) is 62 dB typical, (59 dB max) over temperature; signal to noise and distortion (SINAD) is 60 dB typical; and spurious-free dynamic range (SFDR) is 66 dBFS. Crosstalk is < 75 dB at up to 20 MHz. Providing space, performance, and cost advantages unavailable with separate ICs, the AD10242 is useful in I and Q signal processing, radar and FLIR processing, and secure communications systems.




The AD10242 is manufactured at Analog Devices on our MIL-PRF-38534 line and is completely qualified. Power dissipation is less than 2 watts. Units are packaged in a custom cofired ceramic 68-lead gullwing package and specified for operation from –55 to +125°C. An evaluation board is available. AD10242 prices start at $650 in 1000s. **Faxcode* 2049** A



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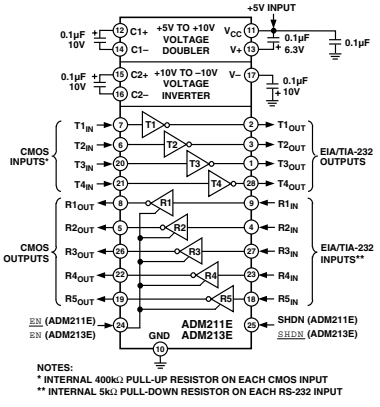
# Transceivers, Switched-Cap Regulator

## EMI/EMC-Compliant RS-232 T-Rs

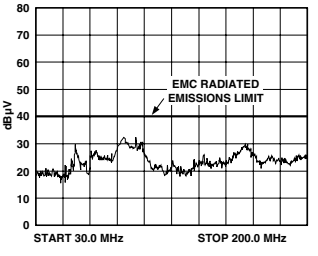
### ADM2xxE Series meet European IEC 1000 specs, Minimal cost, minimal-risk replacement/upgrade

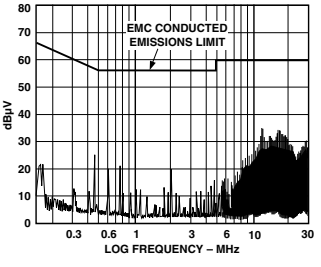



The ADM2xxE series is a family of robust RS-232 and V.28 interface devices that operate from a single +5-V supply. With 230 kbps, they are fast enough for ISDN modem-to-PC connections. These products, suitable for operation in harsh electrical environments, comply with the EU directive on EMC (89/336/EEC) in regard to both emissions and immunity. EM *Immunity* includes ESD protection in excess of ±15 kV on all I/O lines, radiated immunity, and fast transient burst protection (1000-4-2, 3, & 4). *Emissions* include radiated and conducted emissions as required by Information Technology Equipment EN55022, CISPR22.

All devices fully conform to the EIA-232E and CCITTV.28 specifications. The TSSOP package saves up to 40% footprint of existing packages. The table indicates a sampling of available devices, including devices with Shutdown (1 µW) and Enable controls. Shown above is the block diagram of ADM211E. Like all the others, it is an upgrade for existing second sources and is backward compatible with earlier ADM2xx products. They are specified for operation over the range, –40 to +85°C, and are suitable for use in laptop and notebook computers, printers, peripherals, and modems, including ISDN.

**Emissions:** The data sheets for these products discuss the immunity and emissions tests and results in some depth. In the limited space available here, we show examples of radiated and conducted emissions test results. **Circle 7** A



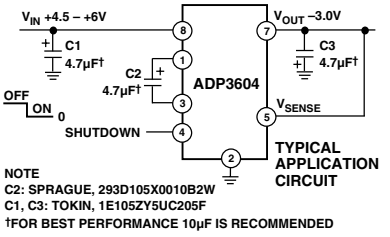




| Characteristic | ADM202E/ ADM1181A | ADM207E | ADM208E | ADM211E | ADM213E |
|---|---|---|---|---|---|
| Supply voltage | +5 V | +5 V | +5 V | +5 V | +5 V |
| Drivers | 2 | 5 | 4 | 4 | 4 |
| Receivers | 2 | 3 | 4 | 5 | 5 |
| ESD Protection | ±15 kV | ±15 kV | ±15 kV | ±15 kV | ±15 kV |
| Shutdown | No | No | No | Yes | Yes ($\overline{SD}$)* |
| $\overline{Enable}$ | No | No | No | Yes | Yes (EN) |
| Packages | N, RW, RN, RU | N, R, RS, RU | N, R, RS, RU | R, RS, RU | R, RS, RU |
| Pins | 16 | 24 | 24 | 28 | 28 |
| Price (1000s) | $1.40 | $2.20 | $2.20 | $2.20 | $2.20 |
| Faxcode | 1992 | 1991 | 1991 | 1991 | 1991 |

*Two receivers active
**Packages: N**: DIP, **R**: SO, **RW**: wide SO, **RN**: narrow SO, **RS**: SSOP, **RU**: TSSOP

## REGULATED DC-DC

### ADP3604 switched-cap inverter: 5 V to –3 V @ 120 mA



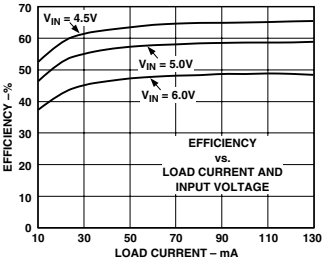

The ADP3604, in an 8-pin SO package, accepts +5-volt dc input and generates a regulated –3-V output at up to 120 mA. It employs capacitor switching at a nominal frequency of 120 kHz, generated by an internal 240-kHz oscillator.

A Shutdown pin allows power to be conserved in battery-powered applications, reducing max supply current by 80%, from 5 mA to 1 mA. Pulling the Shutdown pin high stops the internal oscillator and turns off the output pass transistor.

The specified output range, at 60-mA load, is 3.0 V ±60 mV. For loads from 10 to 120 mA, input voltage from 4.5 to 6 V, and temperature from –40 to +85°C, the output range is 3.0 V±7%. The output load regulation is 0.9 mV/mA for 10 to 40 mA (0.03 Ω) and 1.5 mV/mA for 10 to 120 mA (0.014 Ω).

Typical areas of application include general-purpose voltage inversion and regulation, computer peripherals and add-on cards, portable instruments, battery-powered devices, pagers and radio control receivers, disk drives, and mobile phones.

An evaluation board is available. The ADP3604 operates at temperatures from –40 to +85°C. Price is $2.15 (1000s). **Faxcode* 2051** A



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# Ask The Applications Engineer—22

by Erik Barnes

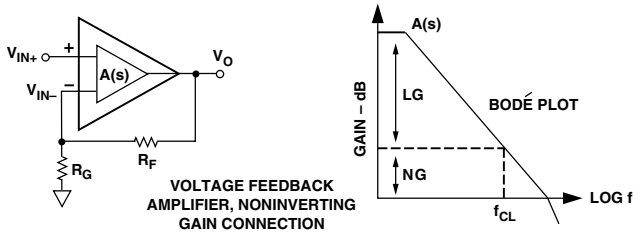
### CURRENT FEEDBACK AMPLIFIERS—I

*Q. I'm not sure I understand how current-feedback amplifiers work as compared with regular op amps. I've heard that their bandwidth is constant regardless of gain. How does that work? Are they the same as transimpedance amplifiers?*

A. Before looking at any circuits, let's define voltage feedback, current feedback, and transimpedance amplifier. *Voltage feedback*, as the name implies, refers to a closed-loop configuration in which the error signal is in the form of a voltage. Traditional op amps use voltage feedback, that is, their inputs will respond to voltage changes and produce a corresponding output voltage. *Current feedback* refers to any closed-loop configuration in which the error signal used for feedback is in the form of a current. A current feedback op amp responds to an error current at one of its input terminals, rather than an error voltage, and produces a corresponding output voltage. Notice that both open-loop architectures achieve the same closed-loop result: zero differential input voltage, and zero input current. The ideal voltage feedback amplifier has high-impedance inputs, resulting in zero input current, and uses voltage feedback to maintain zero input voltage. Conversely, the current feedback op amp has a low impedance input, resulting in zero input *voltage*, and uses current feedback to maintain zero input *current*.

The transfer function of a *transimpedance amplifier* is expressed as a voltage output with respect to a current input. As the function implies, the open-loop "gain", $v_O/i_{IN}$, is expressed in ohms. Hence a current-feedback op amp can be referred to as a *transimpedance amplifier*. It's interesting to note that the closed-loop relationship of a voltage-feedback op amp *circuit* can also be configured as a transimpedance, by driving its dynamically low-impedance summing node with current (e.g., from a photodiode), and thus generating a voltage output equal to that input current multiplied by the feedback resistance. Even more interesting, since ideally any op amp application can be implemented with either voltage or current feedback, this same I-V converter can be implemented with a current feedback op amp. When using the term *transimpedance amplifier*, understand the difference between the specific current-feedback op amp architecture, and any closed-loop I-V converter circuit that acts like transimpedance.

Let's take a look at the simplified model of a voltage feedback amplifier. The noninverting gain configuration amplifies the difference voltage, $(V_{IN+} - V_{IN-})$, by the open loop gain $A(s)$ and feeds a portion of the output back to the inverting input through the voltage divider consisting of $R_F$ and $R_G$. To derive the closed-loop transfer function of this circuit, $V_o/V_{IN+}$, assume




VOLTAGE FEEDBACK AMPLIFIER, NONINVERTING GAIN CONNECTION

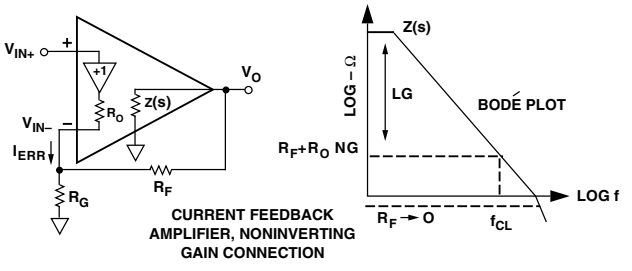
that no current flows into the op amp (infinite input impedance); both inputs will be at about the same potential (negative feedback and high open-loop gain)).

With $V_o = (V_{IN+} - V_{IN-})A(s)$

and

substitute and simplify to get:

The closed-loop bandwidth is the frequency at which the loop gain, $LG$, magnitude drops to unity (0 dB). The term, $1 + R_F/R_G$, is called the *noise gain* of the circuit; for the noninverting case, it is also the signal gain. Graphically, the closed-loop bandwidth is found at the intersection of the open-loop gain, $A(s)$, and the noise gain, NG, in the Bodé plot. High noise gains will reduce the loop gain, and thereby the closed-loop bandwidth. If $A(s)$ rolls off at 20 dB/decade, the gain-bandwidth product of the amplifier will be constant. Thus, an increase in closed-loop gain of 20 dB will reduce the closed-loop bandwidth by one decade.




CURRENT FEEDBACK AMPLIFIER, NONINVERTING GAIN CONNECTION

Consider now a simplified model for a current-feedback amplifier. The noninverting input is the high-impedance input of a unity gain buffer, and the inverting input is its low-impedance output terminal. The buffer allows an error current to flow in or out of the inverting input, and the unity gain forces the inverting input to track the noninverting input. The error current is mirrored to a high impedance node, where it is converted to a voltage and buffered at the output. The high-impedance node is a frequency-dependent impedance, $Z(s)$, analogous to the open-loop gain of a voltage feedback amplifier; it has a high dc value and rolls off at 20 dB/decade.

The closed-loop transfer function is found by summing the currents at the $V_{IN-}$ node, while the buffer maintains $V_{IN+} = V_{IN-}$. If we assume, for the moment, that the buffer has zero output resistance, then $R_o = 0$

Substituting, and solving for $V_o/V_{IN+}$

The closed-loop transfer function for the current feedback amplifier is the same as for the voltage feedback amplifier, but the loop gain $(1/LG)$ expression now depends only on $R_F$, the

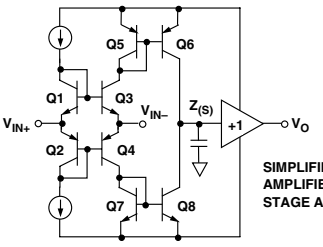
feedback transresistance—and not $(1 + R_F/R_G)$. Thus, the closed-loop bandwidth of a current feedback amplifier will vary with the value of $R_F$, but not with the noise gain, $1 + R_F/R_G$. The intersection of $R_F$ and $Z(s)$ determines the loop gain, and thus the closed-loop bandwidth of the circuit (see Bodé plot). Clearly the gain-bandwidth product is not constant—an advantage of current feedback.

In practice, the input buffer's non-ideal output resistance will be typically about 20 to 40 Ω, which will modify the feedback transresistance. The two input voltages will not be exactly equal. Making the substitution into the previous equations with $V_{IN-} = V_{IN+} - I_{err}R_o$, and solving for $V_o/V_{IN+}$ yields:

The additional term in the feedback transresistance means that the loop gain will actually depend somewhat on the closed-loop gain of the circuit. At low gains, $R_F$ dominates, but at higher gains, the second term will increase and reduce the loop gain, thus reducing the closed-loop bandwidth.

It should be clear that shorting the output back to the inverting input with $R_G$ open (as in a voltage follower) will force the loop gain to get very large. With a voltage feedback amplifier, maximum feedback occurs when feeding back the entire output voltage, but the current feedback's limit is a short-circuit current. The lower the resistance, the higher the current will be. Graphically, $R_F = 0$ will give a higher-frequency intersection of $Z(s)$ and the feedback transresistance—in the region of higher-order poles. As with a voltage feedback amplifier, higher-order poles of $Z(s)$ will cause greater phase shift at higher frequencies, resulting in instability with phase shifts > 180 degrees. Because the optimum value of $R_F$ will vary with closed-loop gain, the Bode plot is useful in determining the bandwidth and phase margin for various gains. A higher closed-loop bandwidth can be obtained at the expense of a lower phase margin, resulting in peaking in the frequency domain, and overshoot and ringing in the time domain. Current-feedback device data sheets will list specific optimum values of $R_F$ for various gain settings.

Current feedback amplifiers have excellent slew-rate capabilities. While it is possible to design a voltage-feedback amplifier with high slew rate, the current-feedback architecture is inherently faster. A traditional voltage-feedback amplifier, lightly loaded, has a slew rate limited by the current available to charge and discharge the internal compensation capacitance. When the input is subjected to a large transient, the input stage will saturate and only its tail current is available to charge or discharge the compensation node. With a current-feedback amplifier, the low-impedance input allows higher transient currents to flow into the amplifier as needed. The internal current mirrors convey this input current to the compensation node, allowing fast charging and discharging—theoretically, in proportion to input step size. A faster slew rate will result in a quicker rise time, lower slew-induced distortion and nonlinearity, and a wider large-signal frequency response. The actual slew rate will be limited by saturation of the current mirrors, which can occur at 10 to 15 mA, and the slew-rate limit of the input and output buffers.




SIMPLIFIED CURRENT FEEDBACK AMPLIFIER, ILLUSTRATING INPUT STAGE AND CURRENT MIRRORS.

*Q. What about dc accuracy?*

A. The dc gain accuracy of a current feedback amplifier can be calculated from its transfer function, just as with a voltage feedback amplifier; it is essentially the ratio of the internal transresistance to the feedback transresistance. Using a typical transresistance of 1 MΩ, a feedback resistor of 1 kΩ, and an $R_o$ of 40 ohms, the gain error at unity gain is about 0.1%. At higher gains, it degrades significantly. Current-feedback amplifiers are rarely used for high gains, particularly when absolute gain accuracy is required.

For many applications, though, the settling characteristics are of more importance than gain accuracy. Although current feedback amplifiers have very fast rise times, many data sheets will only show settling times to 0.1%, because of thermal settling tails— a major contributor to lack of settling precision. Consider the complementary input buffer above, in which the $V_{IN-}$ terminal is offset from the $V_{IN+}$ terminal by the difference in $V_{BE}$ between Q1 and Q3. When the input is at zero, the two $V_{BE}$s should be matched, and the offset will be small from $V_{IN+}$ to $V_{IN-}$. A positive step input applied to $V_{IN+}$ will cause a reduction in the $V_{CE}$ of Q3, decreasing its power dissipation, thus increasing its $V_{BE}$. Diode-connected Q1 does not exhibit a $V_{CE}$ change, so its $V_{BE}$ will not change. Now a different offset exists between the two inputs, reducing the accuracy. The same effect can occur in the current mirror, where a step change at the high-impedance node changes the $V_{CE}$, and thus the $V_{BE}$, of Q6, but not of Q5. The change in $V_{BE}$ causes a current error referred back to $V_{IN-}$, which—multiplied by $R_F$—will result in an output offset error. Power dissipation of each transistor occurs in an area that is too small to achieve thermal coupling between devices. Thermal errors in the input stage can be reduced in applications that use the amplifier in the inverting configuration, eliminating the common-mode input voltage.

*Q. In what conditions are thermal tails a problem?*

A. It depends on the frequencies and waveforms involved. Thermal tails do not occur instantaneously; the thermal coefficient of the transistors (which is process dependent) will determine the time it takes for the temperature change to occur and alter parameters—and then recover. Amplifiers fabricated on the Analog Devices high-speed complementary bipolar (CB) process, for example, don't exhibit significant thermal tails for input frequencies above a few kHz, because the input signal is changing too fast. Communications systems are generally more concerned with spectral performance, so additional gain errors that might be introduced by thermal tails are not important. Step waveforms, such as those found in imaging applications, can be adversely affected by thermal tails when dc levels change. For these applications, current-feedback amplifiers may not offer adequate settling accuracy.

*Part II will consider common application circuits using current-feedback amplifiers and view their operation in more detail.* A

# Worth Reading

### CATALOGS

**1996 SHORT-FORM DESIGNERS' GUIDE** is a **FREE** 228-page complete catalog of Analog Devices products available as of the time of publication. It includes **43 selection trees** to facilitate product searches. There are **48 selection guides** with comparative specifications and other information, and an in-depth **New Products** section. A 21-page **Military/Aerospace** section includes cross-listing of generic part numbers and Standard Military Drawings, plus listings or MIL-STD-883B products, JAN-QPL Class B products, and Space-qualified JAN and non-JAN products. Finally, an **Appendix** includes Package options, Evaluation boards, Power supplies, product families Still Available, Substitution guide, Technical Publications, worldwide Sales directory, and a complete Product Index. **Circle 8**

**DESIGNERS' CD-ROM REFERENCE MANUAL.** This comprehensive CD is now available. It includes Product Selection, Databook, Cross-Reference to competitive part numbers, and a worldwide Sales Directory. **FREE. Circle 9**

### DATA SHEET

**ADSP2106x SHARC DSP Microcomputer Family.** A comprehensive new 44-page data sheet is now available with detailed information about the widely acclaimed 120-MFLOPS peak (80 sustained) SHARC floating-point DSP. For this data sheet, plus development tools data sheet, **ADDS-210xx-TOOLS**, plus Application Note AN-403 (comparing SHARC to a competitive processor), **Circle 10**

### BROCHURE

**Signal Processing for Industrial Applications** is a 14-page summary of Analog Devices's capabilities and components for such applications as industrial Measurement and Process Control, industrial Transmitters, Motor Control, general-purpose PC-based Data Acquisition, and Weigh Scales. **Circle 11**

### APPLICATION NOTES

**Using the AD771x family of 24-bit sigma-delta A/D converters**, by Eamon Nash [12 pp., AN406]. Dealing with frequently raised issues about these high-accuracy converters. **Circle 12**

**AC motor control experiments using the ADMC200-EVAL board**, by Aengus Murray and Paul Kettle [20 pp., AN-407]. Describes a simple motor-control demonstration setup based on the ADMC200 Motion Coprocessor (Analog Dialogue 30-2), interfacing to the ADDS-2101-EZ-LAB digital signal processor board. **Circle 13**

**AC motor control using the ADMC200 coprocessor**, by Aengus Murray and Paul Kettle [8 pp., AN-408]. Describes the design of an ac motor control system using the ADSP-2115 digital signal processor and the ADMC motion coprocessor. **Circle 14**

**Evaluation board for the AD7890, 12-bit serial data-acquisition system**, by Albert O'Grady [6 pp., AN-413]. Describes an evaluation board for the 8-channel AD7890 single-chip data-acquisition system. **Circle 15**

**ADSP-2181 IDMA interface to Motorola MC68300 family of microprocessors**, by ADI Computer Products Division [12 pp., AN-415]. Provides information needed to successfully ntegrate the ADSP-2181 DSP and a controller such as the Motorola MC68300-family into a system. **Circle 16** A

### MORE AUTHORS [*Continued from page 2*]

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**ERRATUM: Analog Dialogue 30-2, page 7, figure 3:** In the left-hand diagram, there should have been dots on the solid line at –3.00 and +3.00 (there are barely perceptible bends at those points) to represent the values for the two missing taps and bring the number of points to 9.

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**PATENTS** • • • 5,519,667 to Stephen Harston for **Random access memory with apparatus for reducing power consumption** • • • 5,485,152 to James Wilson, Ronald Cellini, and James Sobol for **Analog-to-digital conversion using non-uniform sample rates** • • • 5,489,868 to Barrie Gilbert for **Detector cell for logarithmic amplifiers** • • • 5,489,878 to Barrie Gilbert for **Current-controlled quadrature oscillator based on differential $g_m$/C cells** • • • 5,489,903 to James Wilson, Ronald Cellini, and James Sobol for **Digital-to-analog conversion using non-uniform sample rates** • • • 5,497,152 to James Wilson, Ronald Cellini, and James Sobol for **Digital-to-digital conversion using non-uniform sample rates** • • • 5,504,026 to Joseph Kung for **Methods for planarization and encapsulation of micromechanical devices in semiconductor processes** • • • 5,510,156 to Yang Zhao for **Micromechanical structure with textured surface and method for making same** • • • 5,512,897 to James Wilson, Ronald Cellini, and James Sobol for **Variable sample rate DAC** • • • 5,517,123 to Yang Zhao and Richard Payne for **High sensitivity integrated micromechanical electrostatic potential sensor** • • • 5,517,191 to John Wynne for **Digitally controlled calibration circuit for a DAC** • • • 5,519,308 to Barrie Gilbert for **Zero-curvature band gap reference cell** • • • 5,519,354 to Jonathan Audy for **Integrated circuit temperature sensor with programmable offset** • • • 5,519,576 to Thomas Moore for **Thermally enhanced leadframe** • • • 5,519,667 to Stephen Harston for **Random access memory with apparatus for reducing power consumption** • • • 5,521,552 to James Butler for **Bipolar micro-power rail-to-rail amplifier** • • • 5,521,553 to James Butler for **Method for controlling an output stage of a bipolar micro-power rail-to-rail amplifier** • • • 5,521,783 to Edward Wolfe and Andrew Olney for **Electrostatic discharge protection circuit** • • • 5,525,986 to Janos Kovacs, Steven Robinson, and Wyn Palmer for **Intrinsic R2R resistance ladder digital to analog converter** • • • 5,529,939 to Jerome Lapham and Brad Scharf for **Method of making an integrated circuit with complementary isolated bipolar transistors** • • • 5,535,174 to Stephen Harston for **Random access memory with apparatus for reducing power consumption** • • • 5,537,079 to Royal Gosser and Jeffrey Townsend for **Integrated-circuit (IC) amplifier with plural complementary stages**.

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